ARM® Cortex™-M0

32-bit microcontroller

2.4G RF transceiver

HSMicro HS6207™ Series Technical Reference Manual

Version 1.1

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1 HS6207

The HS6207 is a member of the low-cost, high-performance family of intelligent 2.4 GHz RF transceivers with 32bit embedded microcontrollers. The HS6207 is optimized to provide a single chip solution for Ultra Low Power (ULP) wireless applications. The combination of processing power, memory, low power oscillators, real-time counter, and a range of power saving modes provides an ideal platform for implementation of RF protocols.

Benefits of using HS6207 include tighter protocol timing, security, lower power consumption and improved co-existence performance. For the application layer the HS6207 offers a rich set of peripherals including: I2C, UART, PWM,ADC and so on.

1.1 Pin Configuration

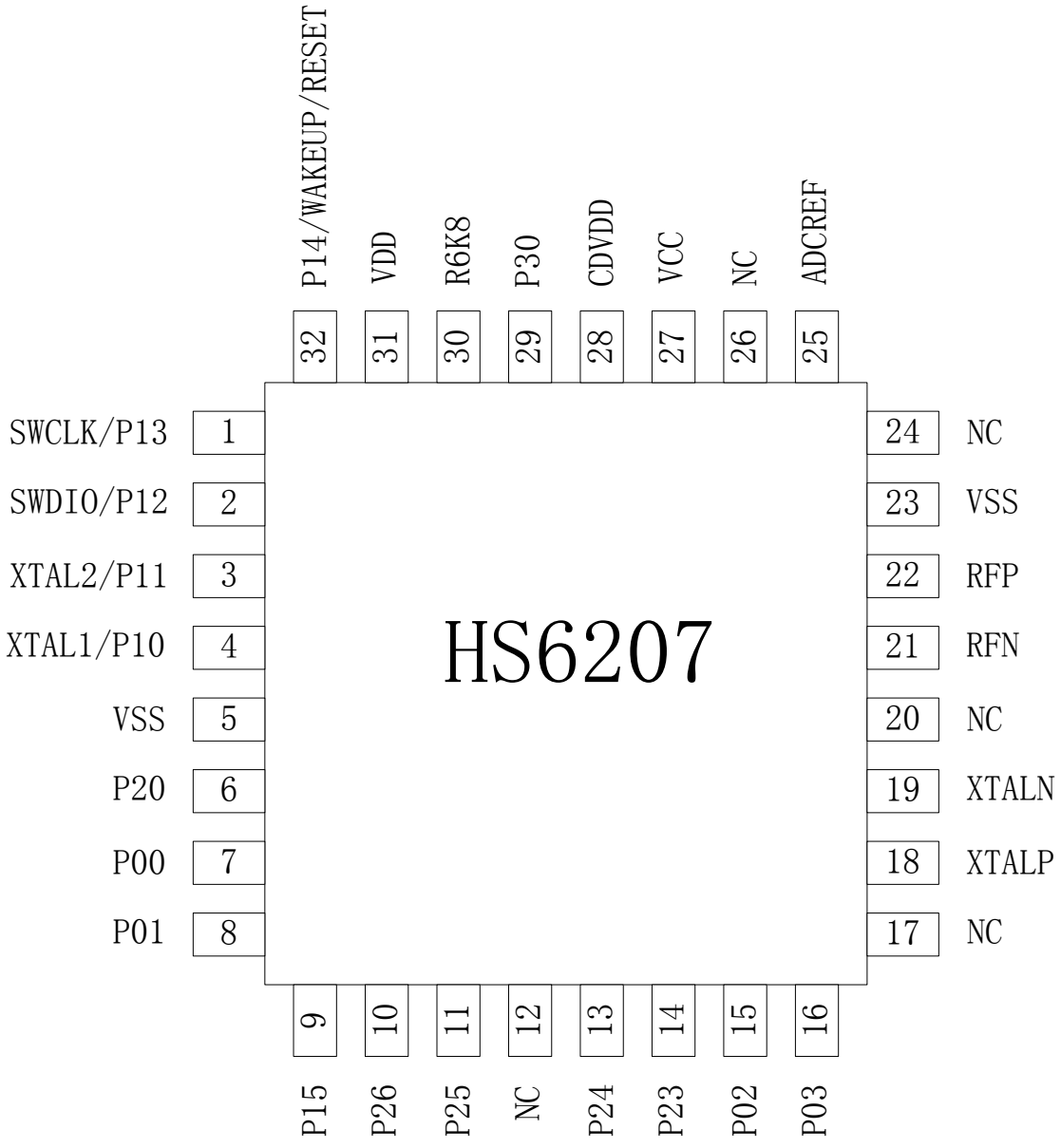


Figure 1.1 Package: 32-pin

1.2 Pin Description

1.2.1 I/O Function

Pin number		Function Symbol							
32	Configuration	0	1	2	3	4	5	6	7
1	SWD_CLK	P13	RXD0	TXD1	RXD2	SDA	SSP_MISO	CTS1	PWM2B
2	SWD_DAT	P12	TXD0	RXD1	TXD2	SCL	SSP_SS	RTS0	PWM2A
3	XTAL2	P11	RXD0	TXD1	RXD2	SDA	SSP_CLK	CTS0	PWM3B
4	XTAL1	P10	TXD0	RXD1	TXD2	SCL	SSP_MOSI	RTS1	PWM3A
5	VSS								
6	SWD_CLK	P20	RXD0	TXD1	RXD2	SDA	SSP_MISO	CTS1	PWM1A
7	SWD_DAT	P00	TXD0	RXD1	TXD2	SCL	SSP_SS	RTS0	PWM0A
8	SWD_CLK	P01	RXD0	TXD1	RXD2	SDA	SSP_CLK	CTS0	PWM0B
9	SWD_DAT	P15	TXD0	RXD1	TXD2	SCL	SSP_MOSI	RTS1	PWM1B
10	SWD_CLK	P26	RXD0	TXD1	RXD2	SDA	SSP_MISO	CTS1	PWM2B
11	SWD_DAT	P25	TXD0	RXD1	TXD2	SCL	SSP_SS	RTS0	PWM2A
12	NC								
13	SWD_DAT	P24	RXD0	TXD1	RXD2	SDA	SSP_CLK	CTS2	PWM3A
14	SWD_CLK	P23	TXD0	RXD1	TXD2	SCL	SSP_MOSI	RTS2	PWM3B
15	SWD_DAT	P02	RXD0	TXD1	RXD2	SDA	SSP_MISO	CTS2	ADC0
16	SWD_CLK	P03	TXD0	RXD1	TXD2	SCL	SSP_SS	RTS2	ADC1
17	NC								
18	XTALP								
19	XTALN								
20	NC								
21	RFN								
22	RFP								
23	VSS								
24	NC								
25	ADCREF								
26	NC								
27	VCC								
28	CDVDD								
29	SWD_CLK	P30	TXD0	RXD1	TXD2	SCL	SSP_SS	RTS2	PWM0A
30	R6K8								
31	VDD								
32	Reset/Wakeup	P14	TXD0	RXD1	TXD2	SCL	SSP_MOSI	RTS1	PWM1A

Table1.2.1 I/O Description

1.2.2 Function Description

Function Symbol	Description
PWMxA	PWM Group x channel A pin.
PWMxB	PWM Group x channel B pin.
TXDx	UART x transmit data pin.
RXDx	UART x receive data pin.
CTSx	Clear to Send input pin for UART x.
RTSx	Request to Send output pin for UART x.
SCL	IIC interface clock pin.
SDA	IIC interface data pin.
SSP_CLK	SSP interface. (SSP clock pin)
SSP_MISO	SSP interface. (Mast - In - Slave - Out)
SSP_MOSI	SSP interface. (Mast - Out - Slave - In)
SSP_SS	SSP interface. (SSP slave select pin)
ADCx	12-bit SAR ADC channel x input pin.
XTALP	Crystal Pin p for RF
XTALN	Crystal Pin n for RF
XTAL2	Crystal Pin 2 for M0
XTAL1	Crystal Pin 1 for M0
RFN	Antenna interface 1
RFP	Antenna interface 2
VSS	
ADCREF	Reference voltage. Connect a 100nFcapacitor to ground.
NC	
VCC	
CDVDD	Internal digital supply output for de-coupling purposes.
R6K8	
VDD	

Table 1.2.2 Function Description

2 MCU

2.1 General Description

The HSMicro HS6207 series are low-cost 32-bit microcontroller with embedded ARM® Cortex™-M0 core for industrial control and applications which need high performance, high-integration low cost requirements.

The HSMicro HS6207 series can run up to 25MHz. The HSMicro HS6207 series provides 28Kbytes embedded program flash, flexibility data flash (Shared with program flash) and fixed 3Kbytes boot code address for the ISP and 2Kbytes embedded SRAM.

Many system level peripheral functions, such as GPIO ports, Timer, UART, SSP, IIC, PWM, Watchdog Timer, 12-bits SAR ADC and low voltage detector, have been incorporated into the HSMicro HS6207 series. The useful functions make the HSMicro HS6207 series powerful for a wide range of applications.

Additionally, the HSMicro HS6207 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the embedded program and data flash without removing the chip from the actual end product.

2.2 Feature

- **Core**
  - ARM® Cortex™-M0 core runs up to 25MHz
  - Built-in Nested Vectored Interrupt Controller (NVIC)
  - Built-in 24-bit system tick timer
  - A single-cycle 32-bit hardware multiplier
  - Supports Serial Wire Debug (SWD) interface and 2 watchpoints / 4 breakpoints
- **Memory**
  - Embedded Flash memory
    - ✓ 28Kbytes on-chip flash memory
    - ✓ Flexibility data flash
    - ✓ Fixed 3 Kbytes boot memory map for ISP application
    - ✓ Minimum 100,000 program/erase cycles
    - ✓ Minimum 10 years data retention
  - 2KByte on-chip SRAM.
- **Clock Control**
  - Programmable system clock source.
  - External crystal input (up to 25Mhz)
  - Internal 22.1184MHz high speed oscillator (+-2% @ 25°C)
  - Internal 10KHz low speed oscillator
- **I/O Port**
  - Up to 25 general-purpose I/O(GPIO) pins
  - I/O pin configuration:
    - ✓ Quasi-bidirectional (Pull-up Enable)
    - ✓ Push-Pull (Output)
    - ✓ Open drain (Pull-up Disable)
    - ✓ Input only (High-impedance)
    - ✓ Analog input for ADC
  - I/O pin can be configured as interrupt source with edge/level setting
  - High ESD: over 8KV
- **Timer**
  - Provides two channel 32/16 bits timer
  - Independent clock source for each timer
  - Selectable One-shot mode, Periodic timer mode or Free-running mode
- **Watchdog Timer**
  - clock source is internal 10KHz
  - 32-bit free running counter
  - Selectable timer-out interval
- **Capture/ PWM**
  - Built-in four 16-bit PWM generators
  - 8-channels PWM output
  - Clock divider for four PWM generator
  - Support 16-bit digital Capture mode with rising/falling/rising to falling/falling to rising capture input
- **UART**
  - Three sets UART interface
  - Compatible with industry-standard 16C450 and 16550A UARTs
  - Programmable baud-rate generator
  - Internal 16 Bytes TXFIFO, 16 Bytes RXFIFO
  - IrDA modulation/Demodulation
- **I2C**
  - One I2C interface
  - Supports master/slave mode
  - Support 7-bit/10-bit addressing

- Support Multi-master
- Programmable clocks allow versatile rate control
- Supports Fast-mode Plus (up to 1 Mbit/s), Fast-mode (up to 400 Kbit/s) and Standard-mode (up to 100 Kbit/s)

➢ **ADC**

- 12-bit SAR ADC with 200ksps
- Up to 8 channel single-ended input.
- Supports single mode/continuous scan mode
- Each channel with an individual result registers

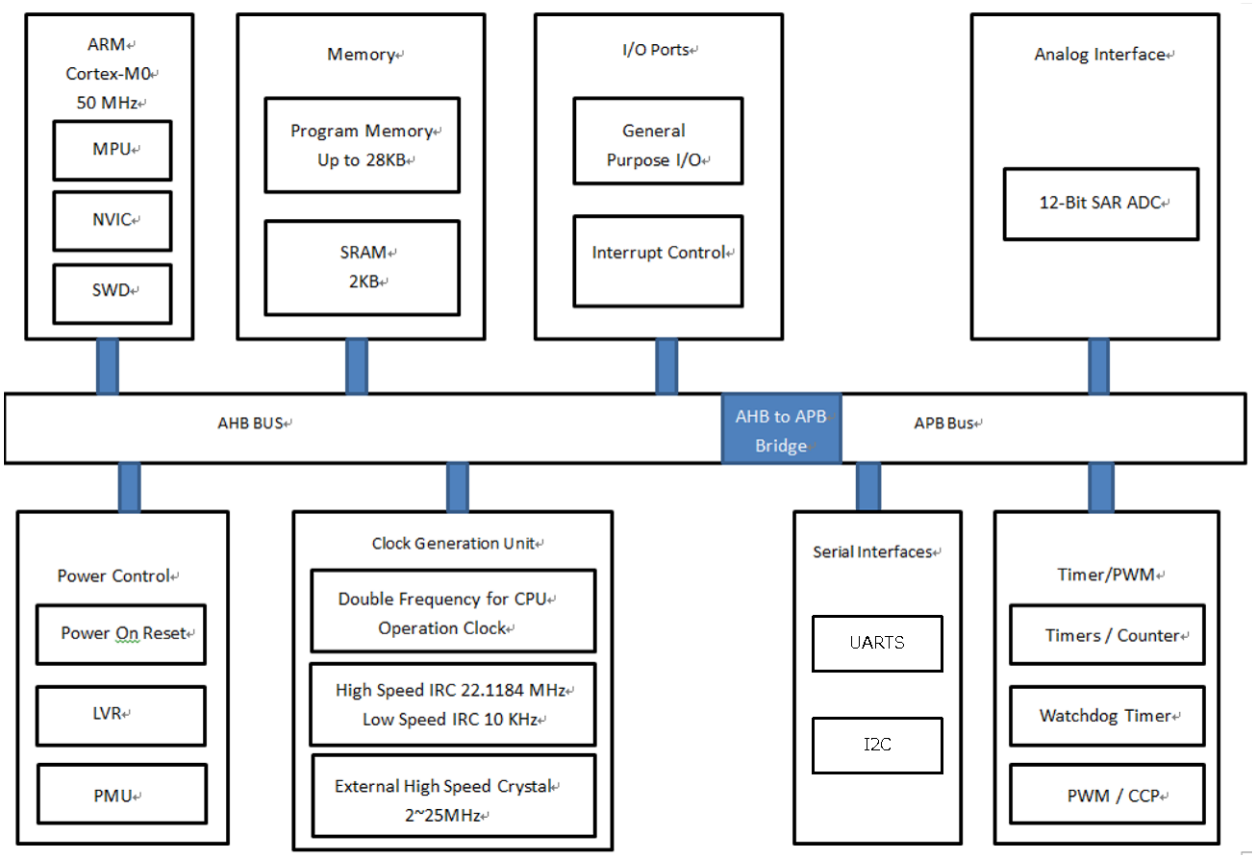
➢ **Flash Memory Controller (FMC)**

- Build-in internal Flash controller for In-Application-Programming (IAP)

➢ **Power Management Unit**

- Support Deep Power down mode
- Support Low speed mode
- Support Sleep mode

2.3 Block Diagram



2.4 Functional Description

2.4.1 ARM® Cortex™-M0 core

The CortexTM - M0 processor is a configurable, multistage, 32-bit RISC processor. It has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex-M profile processors. The profile supports two modes – Thread and Handler modes. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and be entered as a result of an exception return.

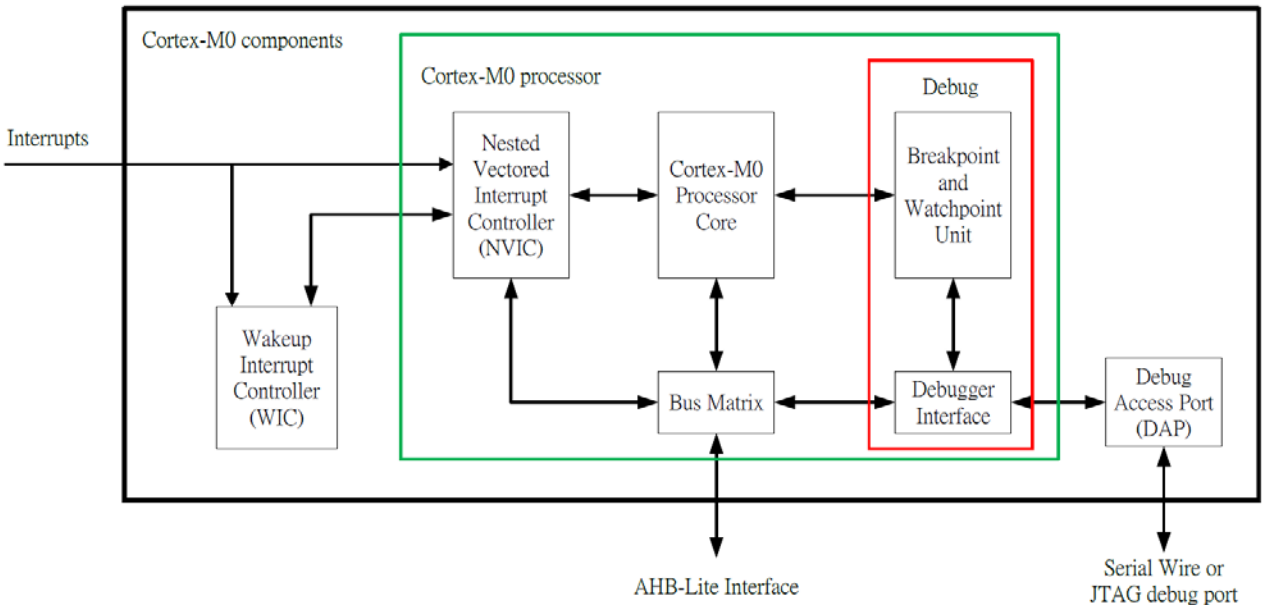


Figure 2.4.1 Cortex-M0 Function Block Diagram

The implemented device provides:

A low gate count processor the features:

- The ARMv6-M Thumb instruction set.
- Thumb-2 technology.
- ARMv6-M compliant 24-bit SysTick timer.
- A 32-bit hardware multiplier. (Single cycle)
- The system interface supports little-endian data accesses.
- The ability to have deterministic, fixed-latency, interrupt handing.
- C Application Binary Interface compliant exception model.

This is the ARMv6-M, C application Binary Interface(C-ABI) compliant exception model that enables

the use of pure C functions as interrupt handlers.

- Low power sleep mode entry using wait for interrupt, wait for event instructions, or the return from interrupt sleep-on-exit feature.

NVIC features:

- 32 external interrupt inputs, each with four levels of priority.
- Dedicated non-Maskable Interrupt (NMI) input.
- Support for both level-sensitive and pulse-sensitive interrupt lines.
- Wake-up Interrupt Controller (WIC), supports ultra-low power sleep mode.

Debug support:

- Four hardware breakpoints.
- Two watch points.
- Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
- Single step and vector catch capabilities.

Bus interface:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
- Single 32-bit slave port that supports the Debug Access Port. (DAP)

2.4.2 **Memory Map**

HSMicro HS6207 series provides a 4G–byte Address space. The memory locations assigned to each on-chip modules are shown as below Table. The detailed register memory addressing and programming will be described in the following sections for individual on-chip peripherals. HSMicro HS6207 series only support little-endian data format.

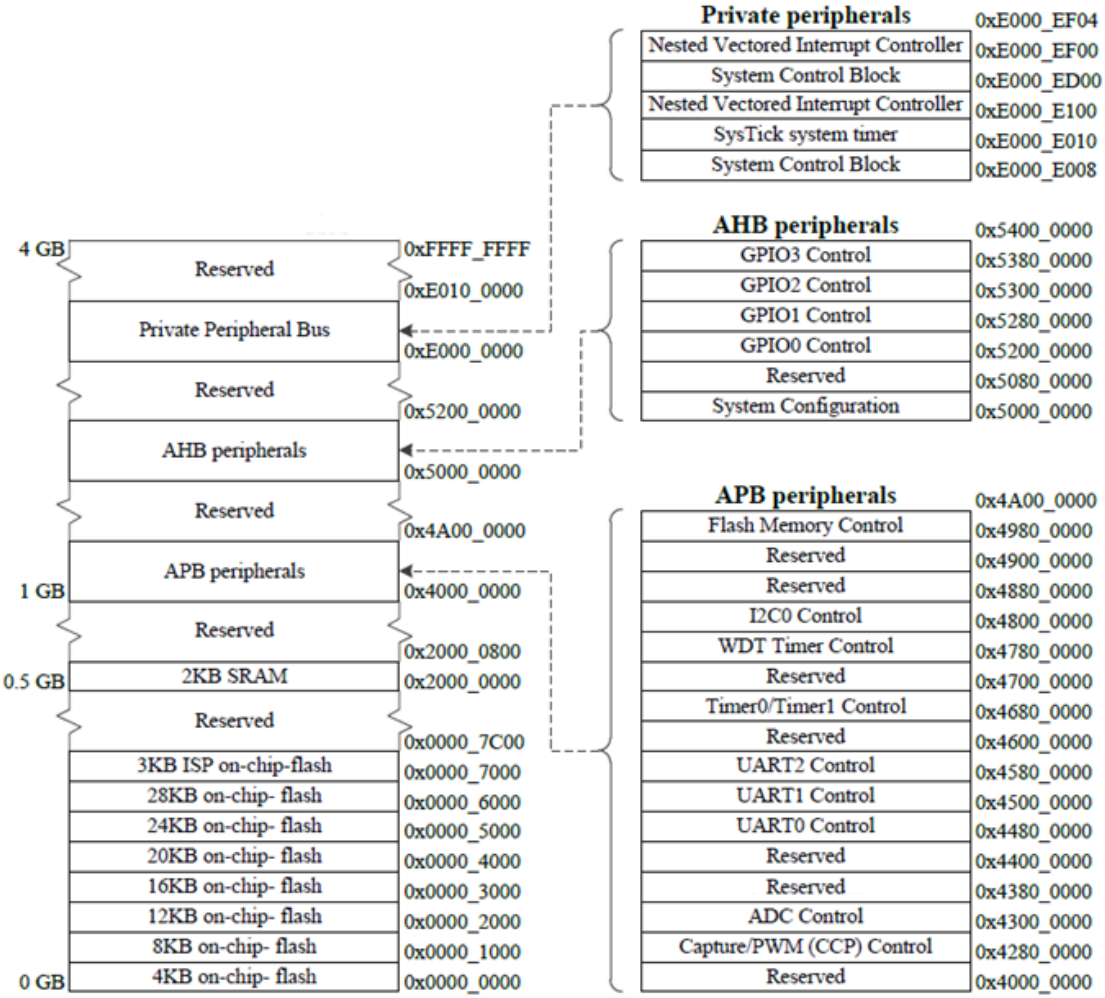


Figure 2.4.2 Memory Map

2.4.3 Watchdog Timer (WDT Base address = 0x4780_0000)

The purpose of Watchdog timer is to perform a system self-reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, Watchdog timer also supports another function to wake up from deep sleep mode.

The watchdog monitors the interrupt and asserts reset signal, when the counter reaches 0, and the counter is stop. On next enable clock edge, the counter is reloaded form the WDTLOAD Register and the countdown sequence continues. If the interrupt is not clear by the time that the counter next reached 0, then timer reasserts the reset signal.

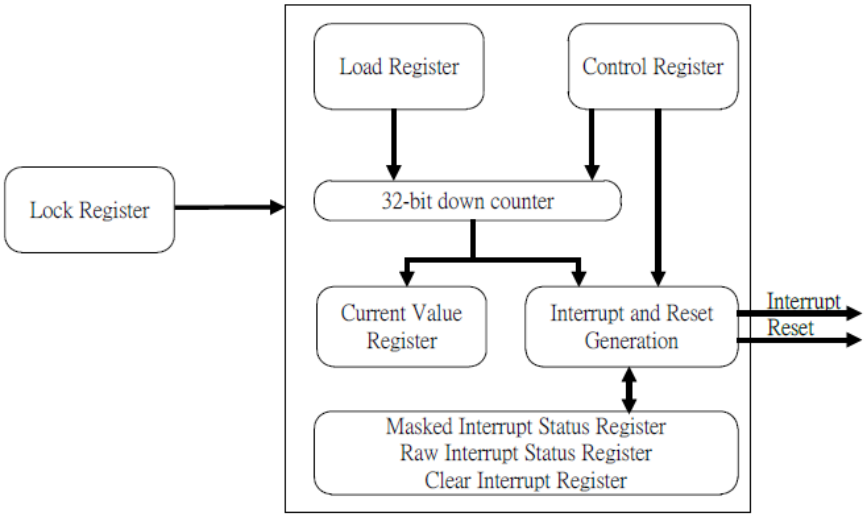


Figure 2.4.3 Watchdog Block Diagram

Name	Offset	Access	Description	Reset value
WDTCON	0x000	R/W	Watchdog Control Register	0x0
WDTLOAD	0x004	R/W	Watchdog Load Register	0xFFFFFFFF
WDTVAL	0x008	RO	Watchdog Current Value Register	0xFFFFFFFF
WDTRIS	0x00C	RO	Watchdog Raw Interrupt Status Register	0x0
WDTMIS	0x010	RO	Watchdog Masked Interrupt Status Register	0x0
WDTICLR	0x014	WO	Watchdog Clear Interrupt Register	-
WDTLOCK	0x500	R/W	Watchdog Lock Register	0x00000000

Table 2.4.3 Register Overview: Watchdog Timer

2.4.3.1 Watchdog Control Register (WDTCON)

Bit	Symbol	Description	Reset value
31:4	-	Reserved, should not write value to the none defined bits	-
3:2	WDTPRE	Watchdog Timer Pre-scale 0x0: Clock is divided by 1 0x1: Clock is divided by 16 0x2: Clock is divided by 256 0x3: Reserved	0
1	WDTRST	Enable Watchdog reset output 0: Disable the reset 1: Enable the reset	0
0	WDTIEN	Enable the interrupt. Reloads the counter from the value in WDTLOAD when the interrupt is enabled, and was previously disabled. 0: Disable the counter and interrupt 1: Enable the counter and the interrupt	0

Table 2.4.3.1 Watchdog Control Register (WDTCON)

2.4.3.2 Watchdog Load Register (WDTLOAD)

Bit	Symbol	Description	Reset value
31:0	WDTLOAD	The WDTLOAD Register is a 32-bit register containing the value from which the counter is to decrement. When this register is written to, the count is immediately restarted from the new value. The minimum valid value for WDTLOAD is 1	0xFFFFFFFF

Table 2.4.3.2 Watchdog Load Register (WDTLOAD)

2.4.3.3 Watchdog Current Value Register (WDTVAL)

Bit	Symbol	Description	Reset value
31:0	WDTVAL	The WDTVAL Register gives the current value of the decrementing counter.	0xFFFFFFFF

Table 2.4.3.3 Watchdog Current Value Register (WDTVAL)

2.4.3.4 Watchdog Raw Interrupt Status Register (WDTRIS)

Bit	Symbol	Description	Reset value
31:1	-	Reserved, should not write value to the none defined bits	-
0	WDTRIS	Raw interrupt status from the counter	0

Table 2.4.3.4 Watchdog Raw Interrupt Status Register (WDTRIS)

2.4.3.5 Watchdog Masked Interrupt Status Register (WDTMIS)

Bit	Symbol	Description	Reset value
31:1	-	Reserved, should not write value to the none defined bits	-
0	WDTMIS	0: Enabled interrupt status from the counter 1: Disable interrupt status from the counter	0

Table 2.4.3.5 Watchdog Masked Interrupt Status Register (WDTMIS)

2.4.3.6 Watchdog Clear Interrupt Register (WDTICLR)

Bit	Symbol	Description	Reset value
31:0	WDTICLR	A write of any value to the WDTICLR Register clears the watchdog interrupt, and reloads the counter from the value in WDTLOAD.	-

Table 2.4.3.6 Watchdog Clear Interrupt Register (WDTICLR)

2.4.3.7 Watchdog Lock Register (WDTLOCK)

Bit	Symbol	Description	Reset value
31:1	WDTKEY	Enable write access to all other registers by writing 0x2AD5334C. Disable write access by writing any other value.	0x0000000
0	WDTREN	Register write enable.	0
		0: Write access to all other registers is disabled	
		1: Write access to all other registers is enabled	

Table 2.4.3.7 Watchdog Lock Register (WDTLOCK)

Note: Unlock by write 0x55AA6699 to WDTLOCK register.

2.4.4 Timer (Timer0 Base address = 0x4680_0000; Timer1 Base address = 0x4680_0100)

HSMicro HS6207 have two programmable 32-bits or 16bits down counter timers, user can easily implement timer control for application. The below modes are available in operation.

Free running mode: The counter wraps after reaching its zero value, and continues to count down from maximum value. The free running mode is default mode.

Periodic timer mode: The counter generates an interrupt at a constant interval, reloading the original value after wrapping past zero.

One-shot timer mode: The counter generates an interrupt once. When the counter reaches 0, it halts until you reprogram it. User can achieve this by either clearing the one-shot count bit in control register, in other case the count proceeds according to the selection of free running or periodic mode or writing new value to the Load value register.

Name	Offset	Access	Description	Reset value
TIMERxCON	0x000	R/W	Timer Control Register	0x20
TIMERxLOAD	0x004	R/W	Timer Load Register	0x00000000
TIMERxVAL	0x008	RO	Timer Current Value Register	0xFFFFFFFF
TIMERxRIS	0x00C	RO	Timer Raw Interrupt Status Register	0x0
TIMERxMIS	0x010	RO	Timer Masked Interrupt Status Register	0x0
TIMERxICLR	0x014	WO	Timer Clear Interrupt Register	-
TIMERxBGLOAD	0x018	R/W	Timer Background Load Register	0x00000000

Table 2.4.4 Register Overview: Timer

2.4.4.1 Timer Control Register (TIMERxCON)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	TMREN	Timer Enable 0: Timer disabled 1: Timer enabled	0
6	TMRMS	Timer Mode Select 0: Timer is in free-running mode 1: Timer is in periodic mode	0
5	TMRIE	Interrupt Enable 0: Timer Interrupt disabled 1: Timer Interrupt enabled	1

4	-	Reserved	-
3:2	TMRPRE	Timer Prescale 00: Clock is divided by 1 01: Clock is divided by 16	0
1	TMRSZ	Selects 16/32 bit counter operation 0: 16-bit counter 1: 32-bit counter	0
0	TMROS	Selects one-shot or wrapping counter mode 0: wrapping mode 1: one-shot mode	0

Table 2.4.4.1 Timer Control Register (TIMERxCON)

2.4.4.2 Timer Load Register (TIMERxLOAD)

Bit	Symbol	Description	Reset value
31:0	TMRxLOAD	When this register is written to directly, the current count is immediately reset to the new value at the next rising edge of TIMER CLK that is enabled by TIMER CLK enable. The value in this register is also overwritten if the TMRXBGLOAD Register is written to, but the current count is not immediately affected. If values are written to both the TMRXLOAD and TMRXBGLOAD Registers before an enabled rising edge on TIMER CLK, the following occurs: 1. On the next enabled TIMER CLK edge, the value written to the TMRXLOAD value replaces the current count value. 2. Then, each time the counter reaches zero, the current count value is reset to the value written to TMRXBGLOAD. Reading from the TMRXLOAD Register at any time after the two writes have occurred retrieves the value written to TMRXBGLOAD. That is, the value read from TMRXLOAD is always the value that takes effect for Periodic mode after the next time the counter reaches zero.	0x00000000

Table 2.4.4.2 Timer Load Register (TIMERxLOAD)

2.4.4.3 Timer Current Value Register (TIMERxVAL)

Bit	Symbol	Description	Reset value
31:0	TMRxVAL	The TMRXVAL Register gives the current value of the decrementing counter.	0xFFFFFFFF

Table 2.4.4.3 Timer Current Value Register (TIMERxVAL)

2.4.4.4 Timer Raw Interrupt Status Register (TIMERxRIS)

Bit	Symbol	Description	Reset value
31:1	-	Reserved, should not write value to the none defined bits	-
0	TMRxRIS	Raw interrupt status from the counter	0

Table 2.4.4.4 Timer Raw Interrupt Status Register (TIMERxRIS)

2.4.4.5 Timer Masked Interrupt Status Register (TIMERxMIS)

Bit	Symbol	Description	Reset value
31:1	-	Reserved, should not write value to the none defined bits	-
0	TMRxMIS	Enabled interrupt status from the counter	0

Table 2.4.4.5 Timer Masked Interrupt Status Register (TIMERxMIS)

2.4.4.6 Timer Clear Interrupt Register (TIMERxICLR)

Bit	Symbol	Description	Reset value
31:0	TMRxICLR	Any write to the TMRXICLR Register clears the interrupt output from the counter.	-

Table 2.4.4.6 Timer Clear Interrupt Register (TIMERxICLR)

2.4.4.7 Timer Background Load Register (TIMERxBGLOAD)

Bit	Symbol	Description	Reset value
31:0	TMRxBGLOAD	The TMRXBGLOAD Register is 32-bits and contains the value from which the counter is to decrement. This is the value used to reload the counter when Periodic mode is enabled, and the current count reaches zero. This register provides an alternative method of accessing the TMRXLOAD Register. The difference is that writes to TMRXBGLOAD do not cause the counter to immediately restart from the new value. Reading from this register returns the same value returned from TMRXLOAD.	0x00000000

Table 2.4.4.7 Timer Background Load Register (TIMERxBGLOAD)

2.4.5 Capture/PWM (PWM Base address = 0x4280_0000)

HSMicro HS6207 series provide four groups for capture function. The capture function input pin channel shared with PWM output channel, each channel support capture on rising/falling edge and count from rising edge to falling edge or count from falling edge to rising edge.

Pulse-width modulation is a digital technique for varying the amount of power delivered to an electronic device. By adjusting the amount of power delivered to a motor or LED, the motor speed and LED brightness can be controlled.

Name	Offset	Access	Description	Reset value
PWMCON0	0x000	R/W	PWM Group 0 Control Register.	0x00
PWMLOAD0	0x004	R/W	PWM Group 0 Load Register.	0x00000
PWMD0A	0x008	R/W	PWM Group 0 Channel A Data Register.	0x00000
PWMD0B	0x00C	R/W	PWM Group 0 Channel B Data Register.	0x00000
PWMCON1	0x010	R/W	PWM Group 1 Control Register.	0x00
PWMLOAD1	0x014	R/W	PWM Group 1 Load Register.	0x00000
PWMD1A	0x018	R/W	PWM Group 1 Channel A Data Register.	0x00000
PWMD1B	0x01C	R/W	PWM Group 1 Channel B Data Register.	0x00000
PWMCON2	0x020	R/W	PWM Group 2 Control Register.	0x00
PWMLOAD2	0x024	R/W	PWM Group 2 Load Register.	0x00000
PWMD2A	0x028	R/W	PWM Group 2 Channel A Data Register.	0x00000
PWMD2B	0x02C	R/W	PWM Group 2 Channel B Data Register.	0x00000
PWMCON3	0x030	R/W	PWM Group 3 Control Register.	0x00
PWMLOAD3	0x034	R/W	PWM Group 3 Load Register.	0x00000
PWMD3A	0x038	R/W	PWM Group 3 Channel A Data Register.	0x00000
PWMD3B	0x03C	R/W	PWM Group 3 Channel B Data Register.	0x00000
PWMIMSC	0x040	R/W	PWM Interrupt Mask Set and Clear Register.	0x00
PWMRIS	0x044	RO	PWM Raw Interrupt Status Register.	0x00
PWMMIS	0x048	RO	PWM Masked Interrupt Status Register.	0x00
PWMICLR	0x04C	WO	PWM Interrupt Clear Register.	0x00
PWMRUN	0x050	R/W	PWM Run Register.	0x0

Table 2.4.5 Register Overview: Capture/PWM

2.4.5.1 PWM Control Register (PWMCONx)

Bit	Symbol	Description	Reset value
31:7	-	Reserved, should not write value to the none defined bits	-
6	PWMEN	PWM Enable 0: Disable 1: Enable	0
5:4	PWMPS	PWM Prescale Select 0x0: PCLK 0x1: PCLK / 4 0x2: PCLK / 16 0x3: PCLK / 64	0x0
3	PWMS	PWM Select 0: Capture Mode 1: PWM Mode.	0
2	CHS	Capture Channel Select 0: Channel A 1: Channel B	0
1:0	CMS	Capture Mode Select 0x0: Capture on rising edge 0x1: Capture on falling edge 0x2: Count from rising edge to falling edge 0x3: Count from falling edge to rising edge	0x0

Table 2.4.5.1 PWM Control Register (PWMCONx)

2.4.5.2 PWM Load Register (PWMLOADx)

Bit	Symbol	Description	Reset value
31:17	-	Reserved, should not write value to the none defined bits	-
16	RELOAD	PWM Reload Enable When RELOAD = '0', Reload Value = 0xFFFF When RELOAD = '1', Reload Value = PWMLOAD	0
15:0	PWMLOAD	PWM Load Value	0x0000

Table 2.4.5.2 PWM Load Register (PWMLOADx)

2.4.5.3 PWM Data Register (PWMDxA/PWMDxB)

Bit	Symbol	Description	Reset value
31:17	-	Reserved, should not write value to the none defined bits	-

16	PWMOP	PWM Output Polarity Select. When PWMOP = '0', PWM leading low output. When PWMOP = '1', PWM leading high output.	0
15:0	PWMDATA	PWM Data	0x0000

Table 2.4.5.3 PWM Data Register (PWMDxA/PWMDxB)

2.4.5.4 PWM Interrupt Mask Set and Clear Register (PWMIMSC)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	PWMIMSC7	PWM Group 3 Overflow Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
6	PWMIMSC6	PWM Group 2 Overflow Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
5	PWMIMSC5	PWM Group 1 Overflow Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
4	PWMIMSC4	PWM Group 0 Overflow Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
3	PWMIMSC3	PWM Group 3 Compare/Capture Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
2	PWMIMSC2	PWM Group 2 Compare/Capture Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
1	PWMIMSC1	PWM Group 1 Compare/Capture Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
0	PWMIMSC0	PWM Group 0 Compare/Capture Interrupt Mask Set and Clear. 0: Disable 1: Enable	0

Table 2.4.5.4 PWM Interrupt Enable Register (PWMIMSC)

2.4.5.5 PWM Raw Interrupt Status Register (PWMRIS)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	PWMRIS7	PWM Group 3 Raw Overflow Interrupt Status	0
6	PWMRIS6	PWM Group 2 Raw Overflow Interrupt Status	0
5	PWMRIS5	PWM Group 1 Raw Overflow Interrupt Status	0
4	PWMRIS4	PWM Group 0 Raw Overflow Interrupt Status	0
3	PWMRIS3	PWM Group 3 Raw Compare/Capture Interrupt Status	0
2	PWMRIS2	PWM Group 2 Raw Compare/Capture Interrupt Status	0
1	PWMRIS1	PWM Group 1 Raw Compare/Capture Interrupt Status	0
0	PWMRIS0	PWM Group 0 Raw Compare/Capture Interrupt Status	0

Table 2.4.5.5 PWM Raw Interrupt Status Register (PWMRIS)

2.4.5.6 PWM Masked Interrupt Status Register (PWMMIS)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	PWMMIS7	PWM Group 3 Masked Overflow Interrupt Status	0
6	PWMMIS6	PWM Group 2 Masked Overflow Interrupt Status	0
5	PWMMIS5	PWM Group 1 Masked Overflow Interrupt Status	0
4	PWMMIS4	PWM Group 0 Masked Overflow Interrupt Status	0
3	PWMMIS3	PWM Group 3 Masked Compare/Capture Interrupt Status	0
2	PWMMIS2	PWM Group 2 Masked Compare/Capture Interrupt Status	0
1	PWMMIS1	PWM Group 1 Masked Compare/Capture Interrupt Status	0
0	PWMMIS0	PWM Group 0 Masked Compare/Capture Interrupt Status	0

Table 2.4.5.6 PWM Masked Interrupt Status Register (PWMMIS)

2.4.5.7 PWM Interrupt Clear Register (PWMICLR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	PWMICLR3	Writing “1” to this bit clears PWM Group 3 Overflow Interrupt Status	0
6	PWMICLR2	Writing “1” to this bit clears PWM Group 2 Overflow Interrupt Status	0

5	PWMICLR1	Writing “1” to this bit clears PWM Group 1 Overflow Interrupt Status	0
4	PWMICLR0	Writing “1” to this bit clears PWM Group 0 Overflow Interrupt Status	0
3	PWMICLR3	Writing “1” to this bit clears PWM Group 3 Compare/Capture Interrupt Status	0
2	PWMICLR2	Writing “1” to this bit clears PWM Group 2 Compare/Capture Interrupt Status	0
1	PWMICLR1	Writing “1” to this bit clears PWM Group 1 Compare/Capture Interrupt Status	0
0	PWMICLR0	Writing “1” to this bit clears PWM Group 0 Compare/Capture Interrupt Status	0

Table 2.4.5.7 PWM Interrupt Clear Register (PWMICLR)

2.4.5.8 PWM Run Register (PWMRUN)

Bit	Symbol	Description	Reset value
31:4	-	Reserved, should not write value to the none defined bits	-
3	PWMRUN3	PWM Group 3 Run. 0: Stop 1: Run	0
2	PWMRUN2	PWM Group 2 Run. 0: Stop 1: Run	0
1	PWMRUN1	PWM Group 1 Run. 0: Stop 1: Run	0
0	PWMRUN0	PWM Group 0 Run. 0: Stop 1: Run	0

Table 2.4.5.8 PWM Run Register (PWMRUN)

2.4.6 Universal Asynchronous Receiver/Transmitter (UART) with modem control (UART0 Base address = 0x4480_0000; UART1 Base address = 0x4500_0000; UART2 Base address = 0x4580_0000)

HSMicro HS6207 series provides three set universal asynchronous receiver/transmitter (UART). UART performs normal speed UART and support flow control function.

The UART baud rate is calculated as:

Baud Rate = PCLK / (16 x DLR)

Name	Offset	Access	Description	Reset value
UARTxRBR	0x000	RO	Receiver Buffer Register. Contains the next received character to be read.	-
UARTxTHR	0x004	WO	Transmit Holding Register. The next character to be transmitted is written here.	-
UARTxDLR	0x008	R/W	Divisor Latch Register. The full divisor is used to generate a baud rate from the fractional rate divider.	0x0001
UARTxIER	0x00C	R/W	Interrupt Enable Register. Contains individual interrupt enable bits for the 7 potential UART interrupts.	0x00
UARTxIIR	0x010	RO	Interrupt Identification Register. Identifies which interrupt(s) are pending.	0x01
UARTxFCR	0x014	WO	FIFO Control Register. Controls UART FIFO usage and modes.	0x00
UARTxLCR	0x018	R/W	Line Control Register. Contains controls for frame formatting and break generation.	0x00
UARTxMCR	0x01C	R/W	Modem control register	0x00
UARTxLSR	0x020	RO	Line Status Register. Contains flags for transmit and receive status, including line errors.	0x60
UARTxMSR	0x024	RO	Modem status register	0x00
UARTxSCR	0x028	R/W	Scratch Pad Register. Eight-bit temporary storage for software.	0x00
UARTxEFR	0x02C	R/W	Enhanced Features Register	0x00
UARTxXON1	0x030	R/W	XON1 Register	0x00
UARTxXON2	0x034	R/W	XON2 Register	0x00
UARTxXOFF1	0x038	R/W	XOFF1 Register	0x00
UARTxXOFF2	0x03C	R/W	XOFF2 Register	0x00

Table 2.4.6 Register Overview: Universal Asynchronous Receiver/Transmitter (UART)

2.4.6.1 UART Receiver Buffer Register (UARTxRBR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	RBR	The UART Receiver Buffer Register contains the oldest received byte in the UART RX FIFO.	-

Table 2.4.6.1 UART Receiver Buffer Register (UARTxRBR)

2.4.6.2 UART Transmitter Holding Register (UARTxTHR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	THR	Writing to the UART Transmit Holding Register causes the data to be stored in the UART transmit FIFO. The byte will be sent when it reaches the bottom of the FIFO and the transmitter is available.	-

Table 2.4.6.2 UART Transmitter Holding Register (UARTxTHR)

2.4.6.3 UART Divisor Latch Register (UARTxDLR)

Bit	Symbol	Description	Reset value
31:16	-	Reserved, should not write value to the none defined bits	-
15:0	DLR	Divisor Latch Register. The full divisor is used to generate a baud rate from the fractional rate divider. Baud rate = PCLK / 16×DLR	0x0001

Table 2.4.6.3 UART Divisor Latch Register (UARTxDLR)

2.4.6.4 UART Interrupt Enable Register (UARTxIER)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-

7	CTSIE	CTS Interrupt Enable. Enable a rising edge is detected on the CTS modem control line. 0: Disable the CTS interrupt. 1: Enable the CTS interrupt.	0
6	RTSIE	RTS Interrupt Enable. Enable a rising edge is detected on the RTS modem control line. 0: Disable the RTS interrupt. 1: Enable the RTS interrupt.	0
5	XOFIE	XOFF Interrupt Enable. Enable an XOFF character is received. 0: Disable the XOF interrupt. 1: Enable the XOF interrupt.	0
4	-	Reserved, should not write value to the none defined bits	-
3	MDSIE	Modem Status Interrupt Enable. 0: Disable the modem status interrupts. 1: Enable the modem status interrupts.	0
2	RLSIE	RX Line Status Interrupt Enable. Enables the UART RX line status interrupts. The status of this interrupt can be read from LSR[4:1]. 0: Disable the RX line status interrupts. 1: Enable the RX line status interrupts.	0
1	THREIE	TX Holding Register Empty Interrupt Enable. Enables the THREIE interrupt for UART. The status of this interrupt can be read from LSR[5]. 0: Disable the THREIE interrupts.	0
0	RBRIE	RX Buffer Register Interrupt Enable. Enables the Receive Data Available interrupt for UART. It also controls the Character Receive Time-out interrupt. 0: Disable the RBRIE interrupts.	0

Table 2.4.6.4 UART Interrupt Enable Register (UARTxIER)

2.4.6.5 UART Interrupt Identification Register (UARTxIIR)

Bit	Symbol	Description	Reset value
31:6	-	Reserved, should not write value to the none defined bits	-

5	INTHFC	Hardware Flow Control (CTS or RTS rising edge) If Set (“1”) indicating that an XOFF character has been received. It is cleared by reading the Interrupt Identification Register.	0
4	INTSFC	Software Flow Control (XOFF character received) If Set (“1”) indicating that a rising edge has been detected on either the RTS/CTS Modem Control line. It is cleared by reading the Interrupt Identification Register.	0
3:1	INTID	Interrupt identification. 0x3: 1 - Receive Line Status. 0x2: 2a - Receive Data Available. 0x6: 2b - Receive FIFO Character Time-out Indicator. 0x1: 3 - TX Holding Register Empty. 0x0: 4 - Modem Status change.	0
0	INT STATUS	Interrupt status. Note that IIR[0] is active low. The pending interrupt can be determined by evaluating IIR[3:1]. 0: At least one interrupt is pending. 1: No interrupt is pending.	1

Table 2.4.6.5 UART Interrupt Identification Register (UARTxIIR)

2.4.6.6 UART FIFO Control Register (UARTxFCR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:6	RXTL	RX Trigger Level. These two bits determine how many receiver UART FIFO characters must be written before an interrupt is activated. 0x0: Trigger level 0 (1 character). 0x1: Trigger level 1 (4 characters). 0x2: Trigger level 2 (8 characters). 0x3: Trigger level 3 (14 characters).	0
5:4	TXTL	TX Trigger Level. These two bits determine how many transmit UART FIFO characters must be written before an interrupt is activated. 0x0: Trigger level 0 (1 character). 0x1: Trigger level 1 (4 characters). 0x2: Trigger level 2 (8 characters). 0x3: Trigger level 3 (14 characters).	0
3	Reserved	Reserved, should not write value to the none defined bits	-

2	TXFIFO RST	TX FIFO Reset 0: No impact on either of UART FIFOs. 1: Writing a logic 1 to FCR[2] will clear all bytes in UART TX FIFO, reset the pointer logic. This bit is self-clearing.	0
1	RXFIFO RST	RX FIFO Reset 0: No impact on either of UART FIFOs. 1: Writing a logic 1 to FCR[1] will clear all bytes in UART RX FIFO, reset the pointer logic. This bit is self-clearing.	0
0	FIFOEN	FIFO Enable 0: UART FIFOs are disabled. Must not be used in the application. 1: Active high enable for both UART RX and TX FIFOs and FCR[7:1] access. This bit must be set for proper UART operation. Any transition on this bit will automatically clear the UART FIFOs.	0

Table 2.4.6.6 UART FIFO Control Register (UARTxFCR)

2.4.6.7 UART Line Control Register (UARTxLCR)

Bit	Symbol	Description	Reset value
31:7	-	Reserved, should not write value to the none defined bits	-
6	BCON	Break Control 0: Disable break transmission. 1: Enable break transmission. Output pin UART TXD is forced to logic 0 when LCR[6] is active high.	0
5:4	PSEL	Parity Select 0x0: Odd parity. Number of 1s in the transmitted character and the attached parity bit will be odd. 0x1: Even Parity. Number of 1s in the transmitted character and the attached parity bit will be even. 0x2: Forced 1 stick parity. 0x3: Forced 0 stick parity.	0
3	PEN	Parity Enable 0: Disable parity generation and checking. 1: Enable parity generation and checking.	0
2	SBS	Stop Bit Select 0: 1 stop bit. 1: 2 stop bits (1.5 if LCR[1:0]=00).	0
1:0	WLS	Word Length Select 0x0: 5-bit character length. 0x1: 6-bit character length. 0x2: 7-bit character length. 0x3: 8-bit character length.	0

Table 2.4.6.7 UART Line Control Register (UARTxLCR)

2.4.6.8 UART Modem Control Register (UARTxMCR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	XOFFS	XOFF Status This read-only bit is set to "1" when an XOFF character is received and cleared when an XON character is received.	0

6	IREN	IrDA mode enables 0: IrDA mode on UART is disabled, 1: IrDA mode on UART is enabled.	0
5	-	Reserved, should not write value to the none defined bits	-
4	MLBM	Modem Loop back mode 0: Disable modem loopback mode. 1: Enable modem loopback mode.	0
3:2	-	Reserved, should not write value to the none defined bits	-
1	RTS	Source for modem output pin RTS. This bit reads as 0 when modem loopback mode is active. 0: Drive RTS pin high.	0

Table 2.4.6.8 UART Modem Control Register (UARTxMCR)

2.4.6.9 UART Line Status Register (UARTxLSR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved.	-
7	RXFE	Error in RX FIFO. LSR[7] is set when a character with a RX error such as framing error, parity error or break interrupt, is loaded into the RBR. This bit is cleared when the LSR register is read and there are no subsequent errors in the UART FIFO. 0: RBR contains no UART RX errors or FCR[0]=0. 1: UART RBR contains at least one UART RX error.	0
6	TEMT	Transmitter Empty. TEMT is set when both THR and TSR are empty; TEMT is cleared when either the TSR or the THR contain valid data. 0: THR and/or the TSR contains valid data. 1: THR and the TSR are empty.	0
5	THRE	Transmitter Holding Register Empty. THRE is set immediately upon detection of an empty UART THR and is cleared on a THR write. 0: THR contains valid data. 1: THR is empty.	0

4	BI	Break Interrupt. When RXD1 is held in the spacing state (all zeros) for one full character transmission (start, data, parity, stop), a break interrupt occurs. Once the break condition has been detected, the receiver goes idle until RXD1 goes to marking state (all ones). A LSR read clears this status bit. The time of break detection is dependent on FCR[0]. Note: The break interrupt is associated with the character at the top of the UART RBR FIFO. 0: Break interrupt status is inactive. 1: Break interrupt status is active.	0
3	FE	Framing Error. When the stop bit of a received character is a logic 0, a framing error occurs. A LSR read clears LSR[3]. The time of the framing error detection is dependent on FCR0. Upon detection of a framing error, the RX will attempt to re-synchronize to the data and assume that the bad stop bit is actually an early start bit. However, it cannot be assumed that the next received byte will be correct even if there is no Framing Error. Note: A framing error is associated with the character at the top of the UART RBR FIFO.	0
2	PE	Parity Error. When the parity bit of a received character is in the wrong state, a parity error occurs. A LSR read clears LSR[2]. Time of parity error detection is dependent on FCR[0]. Note: A parity error is associated with the character at the top of the UART RBR FIFO. 0: Parity error status is inactive. 1: Parity error status is active.	0
1	OE	Overrun Error. The overrun error condition is set as soon as it occurs. A LSR read clears LSR[1]. LSR[1] is set when UART RSR has a new character assembled and the UART RBR FIFO is full. In this case, the UART RBR FIFO will not be overwritten and the character in the UART RSR will be lost. 0: Overrun error status is inactive. 1: Overrun error status is active.	0

0	RDR	Receiver Data Ready: LSR[0] is set when the RBR holds an unread character and is cleared when the UART RBR FIFO is empty. 0: RDR is empty. 1: RDR contains valid data.	0

Table 2.4.6.9 UART Line Status Register (UARTxLSR)

2.4.6.10 UART Modem Status Register (UARTxMSR)

Bit	Symbol	Description	Reset value
31:5	-	Reserved, should not write value to the none defined bits	-
4	CTS	Clear To Send State. Complement of input signal CTS. This bit is connected to MCR[1] in modem loopback mode.	0
3:1	-	Reserved, should not write value to the none defined bits	-
0	DCTS	Delta CTS. Set upon state change of input CTS. Cleared on an MSR	0

Table 2.4.6.10 UART Modem Status Register (UARTxMSR)

2.4.6.11 UART Scratch Pad Register (UARTxSCR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	PAD	A readable, writable byte.	0x00

Table 2.4.6.11 UART Scratch Pad Register (UARTxSCR)

2.4.6.12 UART Enhanced Features Register (UARTxEFR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	AUTOCTS	Enables hardware transmission flow control	0
6	AUTORTS	Enables hardware reception flow control (RTS=0, RTS pin is high)	0
5	-	Reserved.	-

4	MEEN	M16x50 Enhancements Enables	0
3:2	TXSWFC	TX Software Flow Control 0x0: No TX Flow Control 0x1: Transmit XON1/XOFF1 as flow control bytes 0x2: Transmit XON2/XOFF2 as flow control bytes 0x3: Transmit XON1 & XON2 and XOFF1 & XOFF2 as flow control words	0x0
1:0	RXSWFC	RX Software Flow Control 0x0: No RX Flow Control 0x1: Receive XON1/XOFF1 as flow control bytes 0x2: Receive XON2/XOFF2 as flow control bytes 0x3: Receive XON1 & XON2 and XOFF1 & XOFF2 as flow control words	0x0

Table 2.4.6.12 UART Enhanced Features Register (UARTxEFR)

2.4.6.13 UART XON1, XON2 Registers (UARTxXON1/UARTxXON2)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	HXON	hold the XON characters used in software control of transmission and reception	0x00

Table 2.4.6.13 UART XON1, XON2 Registers (UARTxXON1/UARTxXON2)

2.4.6.14 UART XOFF1, XOFF2 Registers (UARTxXOFF1/UARTxXOFF2/UART1XOFF1)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	HXOFF	hold the XOFF characters used in software control of transmission and reception	0x00

Table 2.4.6.14 UART XOFF1, XOFF2 Registers (UARTxXOFF1/UARTxXOFF2/UART1XOFF1)

2.4.7 Inter-Integrated Circuit (I²C) Controller (I2C0 Base address = 0x4800_0000)

The I²C controller support operation in master and slave mode. In master mode, it performs arbitration to allow it to operate in multi-master systems. In salve mode, it can interrupt the processor when it recognizes its own 7-bit or 10-bit address or the general call address. The I²C interface is byte oriented and has four operation modes: master transmitter mode, master receiver mode, slave transmitter mode and slave receiver mode. Data transfer from a master transmitter to a slave device. The first byte transmitted by the master is the slave address, next follows byte of data. The salve returns an ACK bit after each received byte. Data transfer from a slave transmitter to a master device. The slave address byte is transmitted by the master and slave returns an ACK bit, next follows the data bytes transmitted by the salve to master. The master returns an ACK bit after all received bytes other than the last byte. The end of the last byte, a not ACK is returned. The master device generates all of the serial clock pulses and the START and STOP condition. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning if the next series transfer, the I²C bus will not be released.

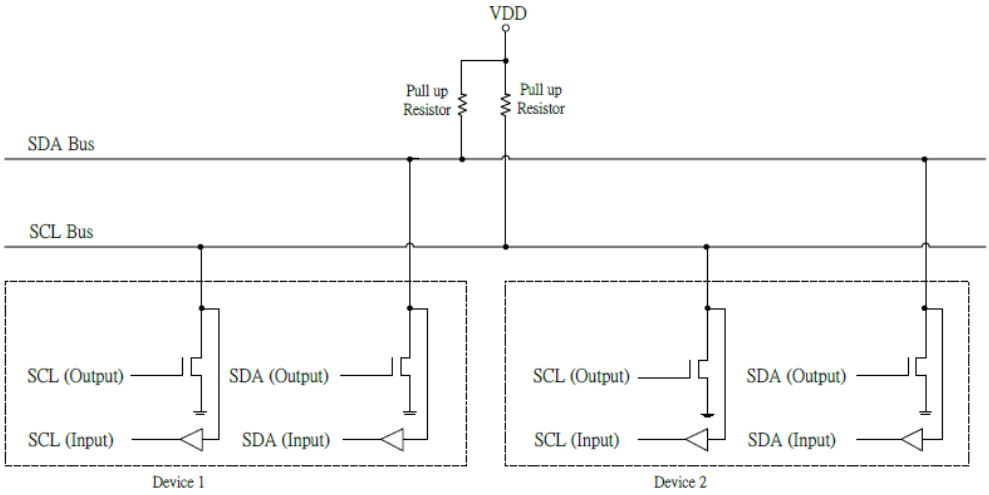


Figure 2.4.7 I²C-Bus Configuration

Name	Offset	Access	Description	Reset value
I2CxCONSET	0x000	R/W	I²C Control Set Register	0x000
I2CxCONCLR	0x004	WO	I²C Control Clear Register	0x00
I2CxSTAT	0x008	RO	I²C Status Register	0xF8
I2CxDAT	0x00C	R/W	I²C Data Register	0x00
I2CxCLK	0x010	R/W	I²C Clock Control Register	0x00
I2CxADR0	0x014	R/W	I²C Slave Address Register 0.	0x00
I2CxADM0	0x018	R/W	I²C Slave Address Mask Register 0.	0xFE
I2CxXADR0	0x01C	R/W	I²C Extended Slave Address Register 0.	0x000
I2CxXADM0	0x020	R/W	I²C Extended Slave Address Mask Register 0.	0x1FE
I2CxRST	0x024	WO	I²C Software Reset Register	0x00
I2CxADR1	0x028	R/W	I²C Slave Address Register 1.	0x00
I2CxADM1	0x02C	R/W	I²C Slave Address Mask Register 1.	0xFE

I2CxADR2	0x030	R/W	I²C Slave Address Register 2.	0x00
I2CxADM2	0x034	R/W	I²C Slave Address Mask Register 2.	0xFE
I2CxADR3	0x038	R/W	I²C Slave Address Register 3.	0x00
I2CxADM3	0x03C	R/W	I²C Slave Address Mask Register 3.	0xFE

Table 2.4.7 Register Overview: Inter-Integrated Circuit (I²C)

2.4.7.1 I²C Control Set Register (I2CxCONSET)

The CONSET register is controls setting of bits in the register that control operation of the I²C interface. There are Bit0 and Bit1 read-only register to read extended salve and salve address FLAG.

Bit	Symbol	Description	Reset value
31:9	-	Reserved, should not write value to the none defined bits	-
8	GCF	I²C General Call FLAG (Read Only) 0: I²C General call address is not match. 1: I²C General call address is match. This bit is clear when new data is transmit/receive.	0
7	I2CIE	Interrupt Enable 0: Disable I²C interrupt. 1: Enable I²C interrupt.	0
6	I2CEN	I²C interface enable. (I2CEN can be cleared by writing 1 to the I2CENC bit in the I2C0CONCLR register.) (The Multi-Function pin function of SDA and SCL must be set to I²C function.) 0: Disable I²C interface. 1: Enable I²C interface.	0
5	STA	START flag. (STA can be cleared by writing 1 to the STAC bit in the I2C0CONCLR register.) When STA is set to one, the I²C enters master mode and will send a START condition on the bus when the bus is free. If the STA bit is set to one when the I²C is already in master mode, then a repeated START condition will be sent. If the STA bit is set to one while the I²C is being	0

		accessed in slave mode, the I²C will complete the data transfer in slave mode then enter master mode when the bus has been released. The STA bit is cleared automatically after a START condition has been sent: writing a zero to this bit has no effect.	
4	STO	STOP flag. If STO is set to one in master mode, a STOP condition is transmitted on the I²C bus. If the STO bit is set to one in slave mode, the I²C will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the I²C bus. If both STA and STO bits are set, the I²C will first transmit the STOP condition (if in master mode) then transmit the START condition. The STO bit is cleared automatically: writing a zero to this bit has no effect.	0
3	SI	I²C interrupt flag. (SI can be cleared by writing 1 to the SIC bit in the I2C0CONCLR register.) This bit is set when the I²C state changes, and if bit I2CIE is set, the I²C interrupt is requested. However, entering state F8 does not set SI since there is nothing for an interrupt service routine to do in that case. The SI is clear by software.	0
2	AA	Assert acknowledge flag. (AA can be cleared by writing 1 to the AAC bit in the I2C0CONCLR register.) (The I²C will not respond as a slave unless AA is set.) 0: A not acknowledge (HIGH level to SDA) will be returned during the acknowledge clock pulse on the SCL line, when a data byte has been received while the I²C is in the master or slave mode. 1: An acknowledge (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line on the following situations: 1. The address in the Slave Address Register has been received. 2. The General Call address has been received while the General Call bit (GC) in the ADR register is set. 3. A data byte has been received while the I²C is in the master or slave mode.	0
1	XADRF	I²C Extended Slave Address FLAG (10-bit addressing) (Read Only) 0: I²C slave address is not match. 1: I²C slave address is match with 10-bit address. This bit is clear when new data is transmit/receive.	0
0	ADRF	I²C Slave Address FLAG (7-bitaddressing) (Read Only) 0: I²C slave address is not match. 1: I²C slave address is match with 7-bit address. This bit is clear when new data is transmit/receive.	0

Table 2.4.7.1 I²C Control Set Register (I2CxCONSET)

2.4.7.2 I²C Control Clear Register (I2CxCONCLR)

The register controls clearing of bit that control operation of the I^2C interface. Writing a one of this register causes the corresponding bit in the I^2C control register to be cleared, writing a zero has no effect.

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	I2CIEC	I^2C interrupt disable. Writing a 1 to this bit clears the I2CIEC bit in the I2C0CONSET register. Writing 0 has no effect.	0
6	I2CENC	I^2C interface disable. Writing a 1 to this bit clears the I2CENC bit in the I2C0CONSET register. Writing 0 has no effect.	0
5	STAC	START flag clear. Writing a 1 to this bit clears the STA bit in the I2C0CONSET register. Writing 0 has no effect.	0
4	-	Reserved, should not write value to the none defined bits	-
3	SIC	I^2C interrupt clear. Writing a 1 to this bit clears the SIC bit in the I2C0CONSET register. Writing 0 has no effect.	0
2	AAC	Assert acknowledge clear. Writing a 1 to this bit clears the AAC bit in the I2C0CONSET register. Writing 0 has no effect.	0
1:0	-	Reserved, should not write value to the none defined bits	-

Table 2.4.7.2 I^2C Control Clear Register (I2CxCONCLR)

2.4.7.3 I²C Status Register (I2CxSTAT)

This register contains a 5-bits status code in the five MSBs; another three LSBs are always zero.

There are 32 possible codes, listed in the table overleaf, 30 of which are status codes and two of which are unused.

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:3	Status	These bits give the actual status information about the I^2C interface.	0x1F
2:0	-	Reserved, should not write value to the none defined bits	-

Table 2.4.7.3.1 I^2C Status Register (I2CxSTAT)

Code	Status
00h	Bus error (Master mode only)
08h	START condition transmitted
10h	Repeated START condition transmitted
18h	Address + Write bit transmitted, ACK received
20h	Address + Write bit transmitted, Not ACK received
28h	Data byte transmitted in master mode, ACK received
30h	Data byte transmitted in master mode, Not ACK received
38h	Arbitration lost in address or data byte
40h	Address + Read bit transmitted, ACK received
48h	Address + Read bit transmitted, Not ACK received
50h	Data byte received in master mode, ACK transmitted
58h	Data byte received in master mode, Not ACK transmitted
60h	Slave address + Write bit received, ACK transmitted
68h	Arbitration lost in address as master, slave address + Write bit received, ACK transmitted
70h	General Call Address received, ACK transmitted
78h	Arbitration lost in address as master, General Call Address received, ACK transmitted
80h	Data byte received after slave address received, ACK transmitted
88h	Data byte received after slave address received, Not ACK transmitted
90h	Data byte received after General Call Address received, ACK transmitted
98h	Data byte received after General Call Address received, Not ACK transmitted
A0h	STOP or repeated START condition received in slave mode
A8h	Slave address + Read bit received, ACK transmitted
B0h	Arbitration lost in address as master, slave address + Read bit received, ACK transmitted
B8h	Data byte transmitted in slave mode, ACK received
C0h	Data byte transmitted in slave mode, Not ACK received
C8h	Last byte transmitted in slave mode, ACK received
D0h	Last byte transmitted in slave mode, Not ACK received
D8h	Unused
E0h	Second Address byte transmitted, ACK received
E8h	Second Address byte transmitted, Not ACK received
F0h	Unused
F8h	No relevant status information, IFLG=0

Table 2.4.7.3.2 I^2C Status Code

2.4.7.4 I²C Data Register (I2CxDAT)

The Register is hold data values that have been received or transmitted.

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	Data	This register holds data values that have been received or are to be transmitted.	0x00

Table 2.4.7.4 I²C Data Register (I2CxDAT)

2.4.7.5 I²C Clock Control Register (I2CxCLK)

Bit	Symbol	Description	Reset value
31:7	-	Reserved, should not write value to the none defined bits	-
6:4	M	FSAMP = PCLK / 2M	0
3:0	N	FSCL = PCLK / (2M×(N+1)×10)	0

Table 2.4.7.5 I²C Clock Control Register (I2CxCLK)

2.4.7.6 I²C Slave Address Registers (I2CxADR0/I2CxADR1/I2CxADR2/I2CxADR3)

The register is readable and writable and is only used when device I²C interface is set to slave mode. In master mode, the register has no effect. The LSB of the address register is the General Call bit. When the bit is set, the General Call address is recognized.

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:1	Address	The I²C device address for slave mode.	0x00
0	GC	General Call enable bit.	0

Table 2.4.7.6 I²C Slave Address Registers (I2CxADR0/I2CxADR1/I2CxADR2/I2CxADR3)

2.4.7.7 I²C Salve Address Mask Registers (I2CxADM0/I2CxADM1/I2CxADM2/I2CxADM3)

The 7 bits registers each contain seven active bits [7:1]. Any bit in these registers which is set to "1" will cause an automatic compare in the corresponding bit for the received address when it

is compared to the address register which are masked are not taken into account in determining an address match.

bits[31:8] and bit[0] of the mask registers are unused and should not be written to. These bits will always read back as “0”.

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:1	MASK	Mask bits. 0: The received corresponding address bit doesn't care. 1: The received corresponding address bit should be exact the same as address register. The mask register has no effect on comparison to the General Call address. When an address-match interrupt occurs, the processor will have to read the data register (DAT) to determine what the received address was that actually caused the match.	0x7F
0	-	Reserved.	-

Table 2.4.7.7 I²C Salve Address Mask Registers (I2CxADM0/I2CxADM1/I2CxADM2/I2CxADM3)

2.4.7.8 I²C Extended Slave Address Registers (I2CxXADR0)

The register is readable and writable and is only used when device I²C interface is set to extended slave mode. In master mode, the register has no effect. The LSB of the address register is the General Call bit. When the bit is set, the General Call address is recognized.

Bit	Symbol	Description	Reset value
31:11	-	Reserved, should not write value to the none defined bits	-
10:1	Address	The I²C device address for slave mode.	0x000
0	GC	General Call enable bit.	0

Table 2.4.7.8 I²C Extended Slave Address Registers (I2CxXADR0)

2.4.7.9 I²C Extended Slave Address Mask Registers (I2CxXADM0)

The 8 bits registers each contain seven active bits (8:1). Any bit in these registers which is set to “1” will cause an automatic compare in the corresponding bit for the received address when it

is compared to the address register which are masked are not taken into account in determining an address match.

Bits (31:9) and bit (0) of the mask registers are unused and should not be written to. These bits will always read back as “0”.

Bit	Symbol	Description	Reset value
31:9	-	Reserved, should not write value to the none defined bits	-
8:1	MASK	Mask bits. 0: The received corresponding address bit is don't care. 1: The received corresponding address bit should be exact the same as address register. The mask register has no effect on comparison to the General Call address. When an address-match interrupt occurs, the processor will have to read the data register (DAT) to determine what the received address was that actually caused the match.	0xFF
0	-	Reserved, should not write value to the none defined bits	-

Table 2.4.7.9 I²C Extended Slave Address Mask Registers (I2CxXADM0)

2.4.7.10 I²C Software Reset Register (I2CxRST)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	RST	I²C software reset by writes 0x07.	0x00

Table 2.4.7.10 I²C Software Reset Register (I2CxRST)

2.4.8 Analog-to-Digital Converter (ADC) (ADC Base address = 0x4300_0000)

HSMicro HS6207 has 12bit Successive Approximation Register (SAR) analog to digital converter and measurement range from 0.01*AVDD to 0.99*AVDD. The analog to digital converter has 8-input source with up to 4096 step resolution to transfer analog signal to digital data.

Note: Please switch pin settings to input mode before ADC enable. (Register GPIOxPMS)

Name	Offset	Access	Description	Reset value
ADCCON	0x000	R/W	A/D Control Register.	0x0
ADCSCAN	0x004	R/W	A/D Scan Register.	0x000
ADCDAT0	0x008	RO	A/D Channel 0 Data Register.	0x000
ADCDAT1	0x00C	RO	A/D Channel 1 Data Register.	0x000
ADCDAT2	0x010	RO	A/D Channel 2 Data Register.	0x000
ADCDAT3	0x014	RO	A/D Channel 3 Data Register.	0x000
ADCDAT4	0x018	RO	A/D Channel 4 Data Register.	0x000
ADCDAT5	0x01C	RO	A/D Channel 5 Data Register.	0x000
ADCDAT6	0x020	RO	A/D Channel 6 Data Register.	0x000
ADCDAT7	0x024	RO	A/D Channel 7 Data Register.	0x000
ADCIMSC	0x028	R/W	A/D Interrupt Mask Set and Clear Register.	0x00
ADCRIS	0x02C	RO	A/D Raw Interrupt Status Register.	0x00
ADCMIS	0x030	RO	A/D Masked Interrupt Status Register.	0x00
ADCICLR	0x034	WO	A/D Interrupt Clear Register.	0x00

Table 2.4.8 Register Overview: Analog-to-Digital Converter (ADC)

2.4.8.1 A/D Control Register (ADCCON)

The register provides bit to select A/D channels be converted, A/D timing and A/D modes.

Bit	Symbol	Description	Reset value
31:5	-	Reserved, should not write value to the none defined bits	-
4	ADCEN	A/D Converter Enable. 0: Disable 1: Enable	0
3	ADCMS	A/D Mode Select. 0: Single cycle scan analog input channel 1~7 1: Continuous scan analog input channel 1~7	0

2:0	ADCDIV	A/D Division. (The maximum clock frequency is 3.2MHz.) FADC = PCLK / 2ADCDIV Sampling Rate = FADC / 16	0

Table 2.4.8.1 A/D Control Register (ADCCON)

2.4.8.2 A/D Scan Register (ADCSCAN)

Bit	Symbol	Description	Reset value
31:9	-	Reserved, should not write value to the none defined bits	-
8	ADCST	A/D Converter Start. (Clear by software when single cycle scan finish) 0: Conversion stop 1: Conversion start	0
7	ADCE7	Analog Input Channel 7 Enable. 0: Disable 1: Enable	0
6	ADCE6	Analog Input Channel 6 Enable. 0: Disable 1: Enable	0
5	ADCE5	Analog Input Channel 5 Enable. 0: Disable 1: Enable	0
4	ADCE4	Analog Input Channel 4 Enable. 0: Disable 1: Enable	0
3	ADCE3	Analog Input Channel 3 Enable. 0: Disable 1: Enable	0
2	ADCE2	Analog Input Channel 2 Enable. 0: Disable 1: Enable	0
1	ADCE1	Analog Input Channel 1 Enable. 0: Disable 1: Enable	0
0	ADCE0	Analog Input Channel 0 Enable. 0: Disable 1: Enable	0

Table 2.4.8.2 A/D Scan Register (ADCSCAN)

2.4.8.3 A/D Channel 0~7 Data Register (ADCDATx)

The register is read only for analog to digital conversion result.

Bit	Symbol	Description	Reset value
31:12	-	Reserved, should not write value to the none defined bits	-
11:0	RSLT	A/D Conversion Result	0

Table 2.4.8.3 A/D Channel 0~7 Data Register (ADCDATx)

2.4.8.4 A/D Interrupt Mask Set and Clear Register (ADCIMSC)

The register is set interrupt mask and clear for each A/D channel.

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	ADCIMSC7	Analog Input Channel 7 Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
6	ADCIMSC6	Analog Input Channel 6 Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
5	ADCIMSC5	Analog Input Channel 5 Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
4	ADCIMSC4	Analog Input Channel 4 Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
3	ADCIMSC3	Analog Input Channel 3 Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
2	ADCIMSC2	Analog Input Channel 2 Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
1	ADCIMSC1	Analog Input Channel 1 Interrupt Mask Set and Clear. 0: Disable 1: Enable	0
0	ADCIMSC0	Analog Input Channel 0 Interrupt Mask Set and Clear. 0: Disable 1: Enable	0

Table 2.4.8.4 A/D Interrupt Mask Set and Clear Register (ADCIMSC)

2.4.8.5 A/D Raw Interrupt Status Register (ADCRIS)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	ADCRIS7	Analog Input Channel 7 Raw Interrupt Status	0
6	ADCRIS6	Analog Input Channel 6 Raw Interrupt Status	0
5	ADCRIS5	Analog Input Channel 5 Raw Interrupt Status	0
4	ADCRIS4	Analog Input Channel 4 Raw Interrupt Status	0
3	ADCRIS3	Analog Input Channel 3 Raw Interrupt Status	0
2	ADCRIS2	Analog Input Channel 2 Raw Interrupt Status	0
1	ADCRIS1	Analog Input Channel 1 Raw Interrupt Status	0
0	ADCRIS0	Analog Input Channel 0 Raw Interrupt Status	0

Table 2.4.8.5 A/D Raw Interrupt Status Register (ADCRIS)

2.4.8.6 A/D Masked Interrupt Status Register (ADCMIS)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	ADCMIS7	Analog Input Channel 7 Masked Interrupt Status	0
6	ADCMIS6	Analog Input Channel 6 Masked Interrupt Status	0
5	ADCMIS5	Analog Input Channel 5 Masked Interrupt Status	0
4	ADCMIS4	Analog Input Channel 4 Masked Interrupt Status	0
3	ADCMIS3	Analog Input Channel 3 Masked Interrupt Status	0
2	ADCMIS2	Analog Input Channel 2 Masked Interrupt Status	0
1	ADCMIS1	Analog Input Channel 1 Masked Interrupt Status	0
0	ADCMIS0	Analog Input Channel 0 Masked Interrupt Status	0

Table 2.4.8.6 A/D Masked Interrupt Status Register (ADCMIS)

2.4.8.7 A/D Interrupt Clear Register (ADCICLR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	ADCICLR7	Writing a 1 to this bit clears Analog Input Channel 7 Interrupt Status	0
6	ADCICLR6	Writing a 1 to this bit clears Analog Input Channel 6 Interrupt Status	0

5	ADCICLR5	Writing a 1 to this bit clears Analog Input Channel 5 Interrupt Status	0
4	ADCICLR4	Writing a 1 to this bit clears Analog Input Channel 4 Interrupt Status	0
3	ADCICLR3	Writing a 1 to this bit clears Analog Input Channel 3 Interrupt Status	0
2	ADCICLR2	Writing a 1 to this bit clears Analog Input Channel 2 Interrupt Status	0
1	ADCICLR1	Writing a 1 to this bit clears Analog Input Channel 1 Interrupt Status	0
0	ADCICLR0	Writing a 1 to this bit clears Analog Input Channel 0 Interrupt Status	0

Table 2.4.8.7 A/D Interrupt Clear Register (ADCICLR)

2.4.9 System Configuration (SYSCON Base address = 0x5000_0000)

Name	Offset	Access	Description	Reset value
DID	0x000	RO	Device Identification Number Register	-
AHBCKDIV	0x004	R/W	AHB CLK Division Register	0x000
APBCKDIV	0x008	R/W	APB CLK Division Register	0x00
APBCKEN	0x00C	R/W	APB CLK Enable Register	0x7FFF
CLKODIV	0x010	R/W	Clock Output pin Division Register	0x000
PCON	0x014	R/W	Power Control Register	0x0
RSTCON	0x018	WO	Reset Control Register	0x00000000
RSTSTAT	0x01C	R/W	Reset Status Register	-
CLKCON	0x020	R/W	Clock Source Control Register	0xF
CLKSEL	0x024	R/W	Clock Source Select Register	0x0
CLKSTAT	0x028	RO	Clock Source Status Register	0x1
APBCKSEL	0x02C	R/W	APB Clock Source Select Register	0x0
IOMUX	0x030	RO	Read from User Configuration IOMUX	-
IOP00CFG	0x040	R/W	GPIO P00 Configuration Register	0x0
IOP01CFG	0x044	R/W	GPIO P01 Configuration Register	0x0
IOP02CFG	0x048	R/W	GPIO P02 Configuration Register	0x0
IOP03CFG	0x04C	R/W	GPIO P03 Configuration Register	0x0
IOP04CFG	0x050	R/W	GPIO P04 Configuration Register	0x0
IOP05CFG	0x054	R/W	GPIO P05 Configuration Register	0x0
IOP06CFG	0x058	R/W	GPIO P06 Configuration Register	0x0
IOP07CFG	0x05C	R/W	GPIO P07 Configuration Register	0x0
IOP10CFG	0x060	R/W	GPIO P10 Configuration Register	0x0
IOP11CFG	0x064	R/W	GPIO P11 Configuration Register	0x0
IOP12CFG	0x068	R/W	GPIO P12 Configuration Register	0x0
IOP13CFG	0x06C	R/W	GPIO P13 Configuration Register	0x0
IOP14CFG	0x070	R/W	GPIO P14 Configuration Register	0x0
IOP15CFG	0x074	R/W	GPIO P15 Configuration Register	0x0
IOP16CFG	0x078	R/W	GPIO P16 Configuration Register	0x0
IOP17CFG	0x07C	R/W	GPIO P17 Configuration Register	0x0
IOP20CFG	0x080	R/W	GPIO P20 Configuration Register	0x0
IOP21CFG	0x084	R/W	GPIO P21 Configuration Register	0x0
IOP22CFG	0x088	R/W	GPIO P22 Configuration Register	0x0
IOP23CFG	0x08C	R/W	GPIO P23 Configuration Register	0x0
IOP24CFG	0x090	R/W	GPIO P24 Configuration Register	0x0
IOP25CFG	0x094	R/W	GPIO P25 Configuration Register	0x0
IOP26CFG	0x098	R/W	GPIO P26 Configuration Register	0x0
IOP27CFG	0x09C	R/W	GPIO P27 Configuration Register	0x0

IOP30CFG	0x0A0	R/W	GPIO P30 Configuration Register	0x0

Table 2.4.9 Register Overview: System Configuration (SYSCON)

2.4.9.1 Device Identification Number Register (DID)

The register could read HS6207 series device ID number.

Bit	Symbol	Description	Reset value
31:16	DNO	Device number.	0x4B02
15:8	Reserved	Reserved. Please Ignore these bits.	-
7:0	DSF	Device Size of Flash Programming memory. 0x04 : for KN02G01A device 0x08 : for KN02G02A device 0x0C : for KN02G03A device 0x10 : for KN02G04A device 0x14 : for KN02G05A device 0x18 : for KN02G06A device 0x1C : for KN02G07A device	-

Table 2.4.9.1 Device Identification Number Register (DID)

2.4.9.2 AHB CLK Division Register (AHBCKDIV)

The “DCE” register control external/internal input clock is double clock to system clock.

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	AHBDIV	System AHB clock divider values 0: HCLK = FSYS 1~255: Divide by 2×DIV (HCLK = FSYS / (2×DIV)).	0x00

Table 2.4.9.2 AHB CLK Division Register (AHBCKDIV)

2.4.9.3 APB CLK Division Register (APBCKDIV)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	APBDIV	System APB clock divider values 0: PCLK = HCLK 1~255: Divide by 2×DIV (PCLK = HCLK / (2×DIV)).	0x00

Table 2.4.9.3 APB CLK Division Register (APBCKDIV)

2.4.9.4 APB CLK Enable Register (APBCKEN)

Bit	Symbol	Description	Reset value
31:13	-	Reserved, should not write value to the none defined bits	-
12	PWMCE	Capture/PWM PCLK Enable 0: Disable 1: Enable	1
11	ADCCE	ADC PCLK Enable 0: Disable 1: Enable	1
10	-	Reserved, should not write value to the none defined bits	-
9	SSP0CE	SSP0 PCLK Enable 0: Disable 1: Enable	1
8	-	Reserved, should not write value to the none defined bits	-
7	I2C0CE	I2C0 PCLK Enable 0: Disable 1: Enable	1
6	-	Reserved, should not write value to the none defined bits	-
5	UART2CE	UART2 PCLK Enable 0: Disable 1: Enable	1
4	UART1CE	UART1 PCLK Enable 0: Disable 1: Enable	1
3	UART0CE	UART0 PCLK Enable 0: Disable 1: Enable	1
2	-	Reserved, should not write value to the none defined bits	-
1	TIMER01CE	TIMER01 PCLK Enable 0: Disable 1: Enable	1
0	WDTCE	WDT PCLK Enable 0: Disable 1: Enable	1

Table 2.4.9.4 APB CLK Enable Register (APBCKEN)

2.4.9.5 Clock Output pin Division Register (CLKODIV)

Bit	Symbol	Description	Reset value
31:9	-	Reserved, should not write value to the none defined bits	-
8	EN	Clock output enable	0
7:0	DIV	Clock output divider values	0x00

Table 2.4.9.5 Clock Output pin Division Register (CLKODIV)

2.4.9.6 Power Control Register (PCON)

Bit	Symbol	Description	Reset value
31:1	DPDKEY	Enable write access to PCON[0] by writing 0x 2AD5334C. Disable write access by writing any other value.	
0	DPDEN	Deep Power Down Enable 0: Disable 1: Enable	0

Table 2.4.9.6 Power Control Register (PCON)

Note: Entry Deep Power Down by write 0x55AA6699 to PCON.

2.4.9.7 Reset Control Register (RSTCON)

Bit	Symbol	Description	Reset value
31:2	RSTKEY	Enable write access to RSTCON[1:0] by writing 0x156A99A6. Disable write access by writing any other value.	0x00000000
1	CPURST	CPU kernel Reset (Set this bit will reset the Cortex-M0 CPU kernel and FMC, but it won't reload Configuration) 0: Normal 1: Reset CPU	0
0	MCURST	MCU Reset 0: Normal 1: Reset MCU, the Cortex-M0 CPU had issued the reset signal to reset the system by software writing 1	0

Table 2.4.9.7 Reset Control Register (RSTCON)

Note: MCU reset by write 0x55AA6699 to RSTCON; CPU reset by write 0x55AA669A to RSTCON.

2.4.9.8 Reset Status Register (RSTSTAT)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2	CPURS	CPU Reset Status 0: No CPU reset detected. 1: CPU reset detected.	0
1	MCURS	MCU Reset Status 0: No MCU reset detected. 1: MCU reset detected.	0
0	WDTRS	WDT Reset Status 0: No WDT reset detected. 1: WDT reset detected.	0

Table 2.4.9.8 Reset Status Register (RSTSTAT)

2.4.9.9 Clock Source Control Register (CLKCON)

Bit	Symbol	Description	Reset value
31:16	KEY	0x5A69 must be written whenever this register is written. If not written as Key, the write operation is ignored and no bits are written into the register.	-
15:5	-	Reserved, should not write value to the none defined bits	-
4	XOSCEN	External OSC Enable 0: Disable 1: Enable	0
3	IRCEN	Internal OSC Enable 0: Disable 1: Enable	1
2:0	IRCSEL	Internal OSC Select 0x0 : 1MHz (20%) 0x1 : 2MHz (20%) 0x2 : 4MHz (20%) 0x3 : 8MHz (20%) 0x4 : 12MHz (20%) 0x5 : 16MHz (20%) 0x6 : 20MHz (20%) 0x7 : 22.1184MHz (2% @ 25℃)	0x7

Table 2.4.9.9 Clock Source Control Register (CLKCON)

2.4.9.10 Clock Source Select Register (CLKSEL)

Bit	Symbol	Description	Reset value
31:16	KEY	0x5A69 must be written whenever this register is written. If not written as Key, the write operation is ignored and no bits are written into the register.	-
15:2	-	Reserved, should not write value to the none defined bits	-
1:0	CLKSEL	Clock Source Select 0x0 : IRC is select 0x1 : XOSC is select 0x2 : IRC 10KHz is select 0x3 : Reserved	0x0

Table 2.4.9.10 Clock Source Select Register (CLKSEL)

2.4.9.11 Clock Source Status Register (CLKSTAT)

Bit	Symbol	Description	Reset value
31:2	-	Reserved, should not write value to the none defined bits	-
1	XOSCSTB	External OSC Status 0: External OSC is not stable or disable. 1: External OSC is stable.	0
0	IRCSTB	Internal OSC Status 0: IRC is not stable or disable. 1: IRC is stable.	1

Table 2.4.9.11 Clock Source Status Register (CLKSTAT)

2.4.9.12 APB Clock Source Select Register (APBCKSEL)

Bit	Symbol	Description	Reset value
31:2	-	Reserved, should not write value to the none defined bits	-
1:0	TMR01SEL	Timer 0/1 Clock Source Select 0x0 : PCLK is select. 0x1 : IRC is select. 0x2 : XOSC is select. 0x3 : IRC 10KHz is select.	0x0

Table2.4.9.12 APB Clock Source Select Register (APBCKSEL)

2.4.9.13 Read from User Configuration IOMUX (IOMUX)

Bit	Symbol	Description	Reset value
31:10	-	Reserved, should not write value to the none defined bits	-
9	XTALPORT	XTAL pin location 0: P1.0/P1.1 assign to GPIO function. 1: P1.0/P1.1 assign to XTAL function.	-
8	RESETPORT	External reset pin location 0: Enable external reset function. When external reset function enable, the reset pin will assign to P14 and P14 GPIO function MUX will disable. 1: Disable external reset function.	-
7:4	SWCLK_PORT	SWDLK pin location 0xF : SWCLK pin assign to P13 and P13 GPIO function select disable. 0xE : SWCLK pin assign to P20 and P20 GPIO function select disable. 0xD : SWCLK pin assign to P01 and P01 GPIO function select disable. 0xC : SWCLK pin assign to P26 and P26 GPIO function select disable. 0xB : SWCLK pin assign to P23 and P23 GPIO function select disable. 0xA : SWCLK pin assign to P03 and P03 GPIO function select disable. 0x9 : SWCLK pin assign to P05 and P05 GPIO function select disable. 0x8 : SWCLK pin assign to P16 and P16 GPIO function select disable. 0x7 : SWCLK pin assign to P07 and P07 GPIO function select disable. 0x6 : SWCLK pin assign to P30 and P30 GPIO function select disable. 0x5 : SWCLK pin assign to P22 and P22 GPIO function select disable. Others : SWCLK function pin disable.	-

3:0	SWDIO_PORT	SWDIO pin location 0xF : SWDIO pin assign to P12 and P12 GPIO function select disable. 0xE : SWDIO pin assign to P00 and P00 GPIO function select disable. 0xD : SWDIO pin assign to P15 and P15 GPIO function select disable. 0xC : SWDIO pin assign to P25 and P25 GPIO function select disable. 0xB : SWDIO pin assign to P24 and P24 GPIO function select disable. 0xA : SWDIO pin assign to P02 and P02 GPIO function select disable. 0x9 : SWDIO pin assign to P04 and P04 GPIO function select disable. 0x8 : SWDIO pin assign to P17 and P17 GPIO function select disable. 0x7 : SWDIO pin assign to P06 and P06 GPIO function select disable. 0x6 : SWDIO pin assign to P27 and P27 GPIO function select disable. 0x5 : SWDIO pin assign to P21 and P21 GPIO function select disable. Others : Disable SWDIO pin function.	-

Table 2.4.9.13 Read from User Configuration IOMUX (IOMUX)

2.4.9.14 GPIO P00 Configuration Register (IOP00CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2:0	IOP00CFG	P0.0 Function Select 0x0 : GPIO 0x1 : TXD0 0x2 : RXD1 0x3 : TXD2 0x4 : SCL 0x5 : SSP_SS 0x6 : RTS0 0x7 : PWM0A	0x0

Table 2.4.9.14 GPIO P00 Configuration Register (IOP00CFG)

2.4.9.15 GPIO P01 Configuration Register (IOP01CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2:0	IOP01CFG	P0.1 Function Select 0x0 : GPIO 0x1 : RXD0 0x2 : TXD1 0x3 : RXD2 0x4 : SDA 0x5 : SSP_CLK 0x6 : CTS0 0x7 : PWM0B	0x0

Table 2.4.9.15 GPIO P01 Configuration Register (IOP01CFG)

2.4.9.16 GPIO P02 Configuration Register (IOP02CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2:0	IOP02CFG	P0.2 Function Select 0x0 : GPIO 0x1 : RXD0 0x2 : TXD1 0x3 : RXD2 0x4 : SDA 0x5 : SSP_MISO 0x6 : CTS2 0x7 : ADC0	0x0

Table 2.4.9.16 GPIO P02 Configuration Register (IOP02CFG)

2.4.9.17 GPIO P03 Configuration Register (IOP03CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-

2:0	IOP03CFG	P0.3 Function Select 0x0 : GPIO 0x1 : TXD0 0x2 : RXD1 0x3 : TXD2 0x4 : SCL 0x5 : SSP_SS 0x6 : RTS2 0x7 : ADC1	0x0

Table 2.4.9.17 GPIO P03 Configuration Register (IOP03CFG)

2.4.9.18 GPIO P10 Configuration Register (IOP10CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2:0	IOP10CFG	P1.0 Function Select 0x0 : GPIO 0x1 : TXD0 0x2 : RXD1 0x3 : TXD2 0x4 : SCL 0x5 : SSP_MOSI 0x6 : RTS1 0x7 : PWM3A	0x0

Table 2.4.9.18 GPIO P10 Configuration Register (IOP10CFG)

2.4.9.19 GPIO P11 Configuration Register (IOP11CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2:0	IOP11CFG	P1.1 Function Select 0x0 : GPIO 0x1 : RXD0 0x2 : TXD1 0x3 : RXD2 0x4 : SDA 0x5 : SSP_CLK 0x6 : CTS0 0x7 : PWM3B	0x0

Table 2.4.9.19 GPIO P11 Configuration Register (IOP11CFG)

2.4.9.20 GPIO P12 Configuration Register (IOP12CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2:0	IOP12CFG	P1.2 Function Select 0x0 : GPIO 0x1 : TXD0 0x2 : RXD1 0x3 : TXD2 0x4 : SCL 0x5 : SSP_SS 0x6 : RTS0 0x7 : PWM2A	0x0

Table 2.4.9.20 GPIO P12 Configuration Register (IOP12CFG)

2.4.9.21 GPIO P13 Configuration Register (IOP13CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2:0	IOP13CFG	P1.3 Function Select 0x0 : GPIO 0x1 : RXD0 0x2 : TXD1 0x3 : RXD2 0x4 : SDA 0x5 : SSP_MISO 0x6 : CTS1 0x7 : PWM2B	0x0

Table 2.4.9.21 GPIO P13 Configuration Register (IOP13CFG)

2.4.9.22 GPIO P14 Configuration Register (IOP14CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-

2:0	IOP14CFG	P1.4 Function Select 0x0 : GPIO 0x1 : TXD0 0x2 : RXD1 0x3 : TXD2 0x4 : SCL 0x5 : SSP_MOSI 0x6 : RTS1 0x7 : PWM1A	0x0

Table 2.4.9.22 GPIO P14 Configuration Register (IOP14CFG)

2.4.9.23 GPIO P15 Configuration Register (IOP15CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2:0	IOP15CFG	P1.5 Function Select 0x0 : GPIO 0x1 : TXD0 0x2 : RXD1 0x3 : TXD2 0x4 : SCL 0x5 : SSP_MOSI 0x6 : RTS1 0x7 : PWM1B	0x0

Table 2.4.9.23 GPIO P15 Configuration Register (IOP15CFG)

2.4.9.24 GPIO P20 Configuration Register (IOP20CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2:0	IOP20CFG	P2.0 Function Select 0x0 : GPIO 0x1 : RXD0 0x2 : TXD1 0x3 : RXD2 0x4 : SDA 0x5 : SSP_MISO 0x6 : CTS1 0x7 : PWM1A	0x0

Table 2.4.9.24 GPIO P20 Configuration Register (IOP20CFG)

2.4.9.25 GPIO P23 Configuration Register (IOP23CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2:0	IOP23CFG	P2.3 Function Select 0x0 : GPIO 0x1 : TXD0 0x2 : RXD1 0x3 : TXD2 0x4 : SCL 0x5 : SSP_MOSI 0x6 : RTS2 0x7 : PWM3B	0x0

Table 2.4.9.25 GPIO P23 Configuration Register (IOP23CFG)

2.4.9.26 GPIO P24 Configuration Register (IOP24CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2:0	IOP24CFG	P2.4 Function Select 0x0 : GPIO 0x1 : RXD0 0x2 : TXD1 0x3 : RXD2 0x4 : SDA 0x5 : SSP_CLK 0x6 : CTS2 0x7 : PWM3A	0x0

Table 2.4.9.26 GPIO P24 Configuration Register (IOP24CFG)

2.4.9.27 GPIO P25 Configuration Register (IOP25CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-

2:0	IOP25CFG	P2.5 Function Select 0x0 : GPIO 0x1 : TXD0 0x2 : RXD1 0x3 : TXD2 0x4 : SCL 0x5 : SSP_SS 0x6 : RTS0 0x7 : PWM2A	0x0

Table 2.4.9.27 GPIO P25 Configuration Register (IOP25CFG)

2.4.9.28 GPIO P26 Configuration Register (IOP26CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2:0	IOP26CFG	P2.6 Function Select 0x0 : GPIO 0x1 : RXD0 0x2 : TXD1 0x3 : RXD2 0x4 : SDA 0x5 : SSP_MISO 0x6 : CTS1 0x7 : PWM2B	0x0

Table 2.4.9.28 GPIO P26 Configuration Register (IOP26CFG)

2.4.9.29 GPIO P30 Configuration Register (IOP30CFG)

Bit	Symbol	Description	Reset value
31:3	-	Reserved, should not write value to the none defined bits	-
2:0	IOP30CFG	P3.0 Function Select 0x0 : GPIO 0x1 : TXD0 0x2 : RXD1 0x3 : TXD2 0x4 : SCL 0x5 : SSP_SS 0x6 : RTS2 0x7 : PWM0A	0x0

Table 2.4.9.29 GPIO P30 Configuration Register (IOP30CFG)

2.4.10 Flash Memory Controller (FMC) (FMC Base address = 0x4980_0000)

Name	Offset	Access	Description	Reset value
FMCCON	0x000	R/W	FMC Control Register.	0x10
FMCADR	0x004	R/W	FMC Address Register.	0x00000000
FMCDAT	0x008	R/W	FMC Data Register.	0x00000000
FMCCMD	0x00C	R/W	FMC Command Register.	0x0
FMCLOCK	0x010	R/W	FMC Lock Register.	0x00000000

Table 2.4.10 Register Overview: Flash Memory Controller (FMC)

2.4.10.1 FMC Control Register (FMCCON)

The register is control FMC boot address mapping and FMC operation

Bit	Symbol	Description	Reset value
31:6	-	Reserved, should not write value to the none defined bits	-
5	FMCB	FMC Busy 0: FMC Normal operation 1: FMC Busy	0
4	FMCE	Flash Boot Address Mapping Enable. 0: Flash mapping is enabled. Boot from 0x0000_7000. 1: Flash mapping is disabled. Boot from 0x0000_0000.	1
3:0	Reserved	Reserved, should not write value to the none defined bits	-

Table 2.4.10.1 FMC Control Register (FMCCON)

2.4.10.2 FMC Address Register (FMCADR)

Bit	Symbol	Description	Reset value
31:29	Reserved	Reserved.	-
28:2	Address[28:2]	It supports word operation.	0x0000000
1:0	Address[1:0]	Keep 2'b00.	0x0

Table 2.4.10.2 FMC Address Register (FMCADR)

2.4.10.3 FMC Data Register (FMCDAT)

Write date to this register before ISP program operation
Read data to this register before ISP read operation

Bit	Symbol	Description	Reset value
31:0	FMCDAT	FMC Data Register.	0x00000000

Table 2.4.10.3 FMC Data Register (FMCDAT)

2.4.10.4 FMC Command Register (FMCCMD)

Bit	Symbol	Description	Reset value
31:3	Reserved	Reserved.	-
2:0	FMCFUNC	FMC Function 0x0: Default 0x1: Flash Read 0x2: Flash Program 0x3: Flash Page Erase (1KBytes/page) 0x6: Erase Flash memory (Except ISP mapping space & User Configuration) 0x7: Erase code flash and User Configuration.	0x0

Table 2.4.10.4 FMC Command Register (FMCCMD)

2.4.10.5 FMC Lock Register (FMCLOCK)

Bit	Symbol	Description	Reset value
31:1	FMCKEY	Enable write access to all other registers by writing 0x2AD5334C. Disable write access by writing any other value.	0x00000000
0	FMCREN	Register write enable 0: Write access to all other registers is disabled 1: Write access to all other registers is enabled	0

Table 2.4.10.5 FMC Lock Register (FMCLOCK)

Note: Unlock by write 0x55AA6699 to FMCLOCK. Flash can't write and erase by FMC in lock mode.

2.4.11 General Purpose I/O (GPIO) (GPIO0 Base address = 0x5200_0000; GPIO1 Base address = 0x5280_0000; GPIO2 Base address = 0x5300_0000; GPIO3 Base address = 0x5380_0000)

HSMicro HS6207 series provide up to 16 General Purpose I/O pins with configurable Quasi-bidirectional, Push-pull, Open drain, high impedance input mode (GPIOxPMS register), and each I/O pin also can serve as interrupt input pin. Interrupt cab be configured on edge trigger or level trigger. (GPIOxITYPE register) The 25 pin are arranged in four group named with Port0, Port1, Port2 and Port3. Each pin is independent and has the corresponding register bits to control the pin mode function and data. When MCU reset, the all GPIO pin stay in Quasi-bidirectional mode and port data register, reset value 0x0000.

Name	Offset	Access	Description	Reset value
GPIOxPMS	0x000	R/W	GPIO x Pin Mode Select Register.	0x0000
GPIOxDOM	0x004	R/W	GPIO x Data Output Write Mask Register.	0x00
GPIOxDO	0x008	R/W	GPIO x Data Output Register.	0xFF
GPIOxDI	0x00C	RO	GPIO x Data Input Register.	-
GPIOxIMSC	0x010	R/W	GPIO x Interrupt Mask Set and Clear Register.	0x00
GPIOxRIS	0x014	RO	GPIO x Raw Interrupt Status Register.	0x00
GPIOxMIS	0x018	RO	GPIO x Masked Interrupt Status Register.	0x00
GPIOxICLR	0x01C	WO	GPIO x Interrupt Clear Register.	0x00
GPIOxITYPE	0x020	R/W	GPIO x Interrupt Type Register.	0x00
GPIOxIVAL	0x024	R/W	GPIO x Interrupt Value Register.	0x00
GPIOxIANY	0x028	R/W	GPIO x Interrupt Any Edge Register.	0x00
GPIOxDIDB	0x02C	R/W	GPIO x Data Input De-bounce Register.	0x00
GPIOxDOSET	0x030	WO	GPIO x Data Output Set Register.	0x00
GPIOxDOCLR	0x034	WO	GPIO x Data Output Clear Register.	0x00

Table 2.4.11 Register Overview: General Purpose I/O (GPIO)

2.4.11.1 GPIO x Pin Mode Select Register (GPIOxPMS)

The registers are select I/O mode as Quasi-bidirectional, push pull, open drain and input only mode.

Bit	Symbol	Description	Reset value
31:16	-	Reserved, should not write value to the none defined bits	-
15:14	PMS7	Px.7 Select function mode for GPIO 0x0: Quasi-bidirectional (Pull-up Enable) 0x1: Push-pull (Output) 0x2: Open drain (Pull-up Disable) 0x3: Input only or ADC input (High-impedance)	0x0

13:12	PMS6	Px.6 Select function mode for GPIO 0x0: Quasi-bidirectional (Pull-up Enable) 0x1: Push-pull (Output) 0x2: Open drain (Pull-up Disable) 0x3: Input only or ADC input (High-impedance)	0x0
11:10	PMS5	Px.5 Select function mode for GPIO 0x0: Quasi-bidirectional (Pull-up Enable) 0x1: Push-pull (Output) 0x2: Open drain (Pull-up Disable) 0x3: Input only or ADC input (High-impedance)	0x0
9:8	PMS4	Px.4 Select function mode for GPIO 0x0: Quasi-bidirectional (Pull-up Enable) 0x1: Push-pull (Output) 0x2: Open drain (Pull-up Disable) 0x3: Input only or ADC input (High-impedance)	0x0
7:6	PMS3	Px.3 Select function mode for GPIO 0x0: Quasi-bidirectional (Pull-up Enable) 0x1: Push-pull (Output) 0x2: Open drain (Pull-up Disable) 0x3: Input only or ADC input (High-impedance)	0x0
5:4	PMS2	Px.2 Select function mode for GPIO 0x0: Quasi-bidirectional (Pull-up Enable) 0x1: Push-pull (Output) 0x2: Open drain (Pull-up Disable) 0x3: Input only or ADC input (High-impedance)	0x0
3:2	PMS1	Px.1 Select function mode for GPIO 0x0: Quasi-bidirectional (Pull-up Enable) 0x1: Push-pull (Output) 0x2: Open drain (Pull-up Disable) 0x3: Input only or ADC input (High-impedance)	0x0
1:0	PMS0	Px.0 Select function mode for GPIO 0x0: Quasi-bidirectional (Pull-up Enable) 0x1: Push-pull (Output) 0x2: Open drain (Pull-up Disable) 0x3: Input only (High-impedance)	0x0

Table 2.4.11.1 GPIO x Pin Mode Select Register (GPIOxPMS)

Note: The external pull up resistor is necessary in open drain mode. The digital output mode of I/O pin only support sink current capability, so the open drain output high is driven by external pull up resistor.

2.4.11.2 GPIO x Data Output Write Mask Register (GPIOxDOM)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	DOM	Data Output Write Mask Register. 0 = GPIOxDO is not masked. 1 = GPIOxDO is masked. DO is not changed by write GPIOxDO.	0x00

Table 2.4.11.2 GPIO x Data Output Write Mask Register (GPIOxDOM)

2.4.11.3 GPIO x Data Output Register (GPIOxDO)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	DO	Data Output Register. DO can be set by writing 1 to the DO in the GPIOxDO register, clear by writing 0 to the DO in the GPIOxDO register. User can read this register get the data output. Write: 0 = Clear to low. 1 = Set to high. Read: 0 = Low. 1 = High.	0xFF

Table 2.4.11.3 GPIO x Data Output Register (GPIOxDO)

2.4.11.4 GPIO x Data Input Register (GPIOxDI)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	DI	Data Input Register.	0x00

Table 2.4.11.4 GPIO x Data Input Register (GPIOxDI)

2.4.11.5 GPIO x Interrupt Mask Set and Clear Register (GPIOxIMSC)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-

7	IMSC7	Px.7 Interrupt Mask Set and Clear Register 0: Disable 1: Enable	0
6	IMSC6	Px.6 Interrupt Mask Set and Clear Register 0: Disable 1: Enable	0
5	IMSC5	Px.5 Interrupt Mask Set and Clear Register 0: Disable 1: Enable	0
4	IMSC4	Px.4 Interrupt Mask Set and Clear Register 0: Disable 1: Enable	0
3	IMSC3	Px.3 Interrupt Mask Set and Clear Register 0: Disable 1: Enable	0
2	IMSC2	Px.2 Interrupt Mask Set and Clear Register 0: Disable 1: Enable	0
1	IMSC1	Px.1 Interrupt Mask Set and Clear Register 0: Disable 1: Enable	0
0	IMSC0	Px.0 Interrupt Mask Set and Clear Register 0: Disable 1: Enable	0

Table 2.4.11.5 GPIO x Interrupt Mask Set and Clear Register (GPIOxIMSC)

2.4.11.6 GPIO x Raw Interrupt Status Register (GPIOxRIS)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	RIS7	Px.7 Raw Interrupt Status	0
6	RIS6	Px.6 Raw Interrupt Status	0
5	RIS5	Px.5 Raw Interrupt Status	0
4	RIS4	Px.4 Raw Interrupt Status	0
3	RIS3	Px.3 Raw Interrupt Status	0
2	RIS2	Px.2 Raw Interrupt Status	0
1	RIS1	Px.1 Raw Interrupt Status	0
0	RIS0	Px.0 Raw Interrupt Status	0

Table 2.4.11.6 GPIO x Raw Interrupt Status Register (GPIOxRIS)

2.4.11.7 GPIO x Masked Interrupt Status Register (GPIOxMIS)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	MIS7	Px.7 Masked Interrupt Status	0
6	MIS6	Px.6 Masked Interrupt Status	0
5	MIS5	Px.5 Masked Interrupt Status	0
4	MIS4	Px.4 Masked Interrupt Status	0
3	MIS3	Px.3 Masked Interrupt Status	0
2	MIS2	Px.2 Masked Interrupt Status	0
1	MIS1	Px.1 Masked Interrupt Status	0
0	MIS0	Px.0 Masked Interrupt Status	0

Table 2.4.11.7 GPIO x Masked Interrupt Status Register (GPIOxMIS)

2.4.11.8 GPIO x Interrupt Clear Register (GPIOxICLR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	ICLR7	Writing a 1 to this bit clears Px.7 Interrupt Status	0
6	ICLR6	Writing a 1 to this bit clears Px.6 Interrupt Status	0
5	ICLR5	Writing a 1 to this bit clears Px.5 Interrupt Status	0
4	ICLR4	Writing a 1 to this bit clears Px.4 Interrupt Status	0
3	ICLR3	Writing a 1 to this bit clears Px.3 Interrupt Status	0
2	ICLR2	Writing a 1 to this bit clears Px.2 Interrupt Status	0
1	ICLR1	Writing a 1 to this bit clears Px.1 Interrupt Status	0
0	ICLR0	Writing a 1 to this bit clears Px.0 Interrupt Status	0

Table 2.4.11.8 GPIO x Interrupt Clear Register (GPIOxICLR)

2.4.11.9 GPIO x Interrupt Type Register (GPIOxITYPE)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	ITYPE7	Px.7 Interrupt Type Register. 0: Edge trigger 1: Level trigger	0
6	ITYPE6	Px.6 Interrupt Type Register. 0: Edge trigger 1: Level trigger	0

5	ITYPE5	Px.5 Interrupt Type Register. 0: Edge trigger 1: Level trigger	0
4	ITYPE4	Px.4 Interrupt Type Register. 0: Edge trigger 1: Level trigger	0
3	ITYPE3	Px.3 Interrupt Type Register. 0: Edge trigger 1: Level trigger	0
2	ITYPE2	Px.2 Interrupt Type Register. 0: Edge trigger 1: Level trigger	0
1	ITYPE1	Px.1 Interrupt Type Register. 0: Edge trigger 1: Level trigger	0
0	ITYPE0	Px.0 Interrupt Type Register. 0: Edge trigger 1: Level trigger	0

Table 2.4.11.9 GPIO x Interrupt Type Register (GPIOxITYPE)

2.4.11.10 GPIO x Interrupt Value Register (GPIOxIVAL)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	IVAL7	Px.7 Interrupt Trigger Value. 0: Level 0 trigger or Falling edge 1: Level 1 trigger or Rising edge	0
6	IVAL6	Px.6 Interrupt Trigger Value. 0: Level 0 trigger or Falling edge 1: Level 1 trigger or Rising edge	0
5	IVAL5	Px.5 Interrupt Trigger Value. 0: Level 0 trigger or Falling edge 1: Level 1 trigger or Rising edge	0
4	IVAL4	Px.4 Interrupt Trigger Value. 0: Level 0 trigger or Falling edge 1: Level 1 trigger or Rising edge	0
3	IVAL3	Px.3 Interrupt Trigger Value. 0: Level 0 trigger or Falling edge 1: Level 1 trigger or Rising edge	0

2	IVAL2	Px.2 Interrupt Trigger Value. 0: Level 0 trigger or Falling edge 1: Level 1 trigger or Rising edge	0
1	IVAL1	Px.1 Interrupt Trigger Value. 0: Level 0 trigger or Falling edge 1: Level 1 trigger or Rising edge	0
0	IVAL0	Px.0 Interrupt Trigger Value. 0: Level 0 trigger or Falling edge 1: Level 1 trigger or Rising edge	0

Table 2.4.11.10 GPIO x Interrupt Value Register (GPIOxIVAL)

2.4.11.11 GPIO x Interrupt Any Edge Register (GPIOxIANY)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	IANY7	Px.7 Interrupt Trigger Any Edge. 0: Falling or Rising edge depended on GPIOxIVAL7 1: Any edge can trigger	0
6	IANY6	Px.6 Interrupt Trigger Any Edge. 0: Falling or Rising edge depended on GPIOxIVAL6 1: Any edge can trigger	0
5	IANY5	Px.5 Interrupt Trigger Any Edge. 0: Falling or Rising edge depended on GPIOxIVAL5 1: Any edge can trigger	0
4	IANY4	Px.4 Interrupt Trigger Any Edge. 0: Falling or Rising edge depended on GPIOxIVAL4 1: Any edge can trigger	0
3	IANY3	Px.3 Interrupt Trigger Any Edge. 0: Falling or Rising edge depended on GPIOxIVAL3 1: Any edge can trigger	0
2	IANY2	Px.2 Interrupt Trigger Any Edge. 0: Falling or Rising edge depended on GPIOxIVAL2 1: Any edge can trigger	0
1	IANY1	Px.1 Interrupt Trigger Any Edge. 0: Falling or Rising edge depended on GPIOxIVAL1 1: Any edge can trigger	0
0	IANY0	Px.0 Interrupt Trigger Any Edge. 0: Falling or Rising edge depended on GPIOxIVAL0 1: Any edge can trigger	0

Table 2.4.11.11 GPIO x Interrupt Any Edge Register (GPIOxIANY)

2.4.11.12 GPIO x Data Input De-bounce Register (GPIOxDIDB)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7	DIDB7	Px.7 Input De-bounce 0: The Input data is directly from the pin 1: There will be two stages DFF filter	0
6	DIDB6	Px.6 Input De-bounce 0: The Input data is directly from the pin 1: There will be two stages DFF filter	0
5	DIDB5	Px.5 Input De-bounce 0: The Input data is directly from the pin 1: There will be two stages DFF filter	0
4	DIDB4	Px.4 Input De-bounce 0: The Input data is directly from the pin 1: There will be two stages DFF filter	0
3	DIDB3	Px.3 Input De-bounce 0: The Input data is directly from the pin 1: There will be two stages DFF filter	0
2	DIDB2	Px.2 Input De-bounce 0: The Input data is directly from the pin 1: There will be two stages DFF filter	0
1	DIDB1	Px.1 Input De-bounce 0: The Input data is directly from the pin 1: There will be two stages DFF filter	0
0	DIDB0	Px.0 Input De-bounce 0: The Input data is directly from the pin 1: There will be two stages DFF filter	0

Table 2.4.11.12 GPIO x Data Input De-bounce Register (GPIOxDIDB)

2.4.11.13 GPIO x Data Output Set Register (GPIOxDOSET)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	DOS	Data Output Set Register. DO can be set by writing 1 to the DO in the GPIOxDOSET register. Writing a zero to this bit has no effect. Write: 0 = no effect 1 = Set to high.	0x00

Table 2.4.11.13 GPIO x Data Output Set Register (GPIOxDOSET)

2.4.11.14 GPIO x Data Output Clear Register (GPIOxDOCLR)

Bit	Symbol	Description	Reset value
31:8	-	Reserved, should not write value to the none defined bits	-
7:0	DOC	Data Output Clear Register. DO can be cleared by writing 1 to the DOC in the GPIOxDOCLR register. Writing a zero to this bit has no effect. Write: 0 = no effect 1 = Clear to low.	0x00

Table 2.4.11.14 GPIO x Data Output Clear Register (GPIOxDOCLR)

2.4.11.15 Quasi-bidirectional mode (pull-up resistor enabled)

Set GPIOxPMS register to 0x0 the Pin (n) in Quasi-bidirectional mode the I/O pin supports digital output and input function at the same time.

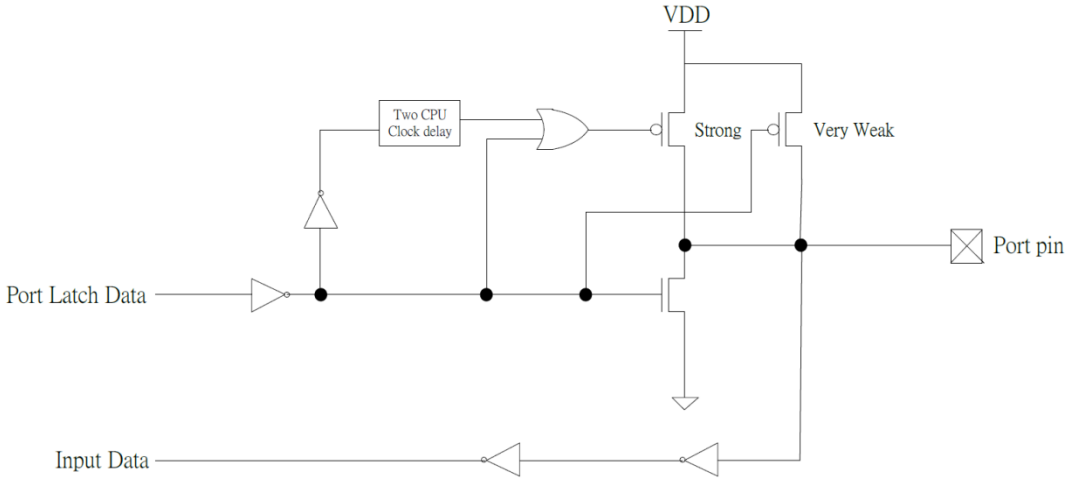


Figure 2.4.11.15 Quasi-bidirectional mode (pull-up resistor enabled)

2.4.11.16 Push-pull mode (Output)

Set GPIOxPMS register to 0x1 the Pin (n) in output mode, the I/O pin supports digital output with source/sink current capability.

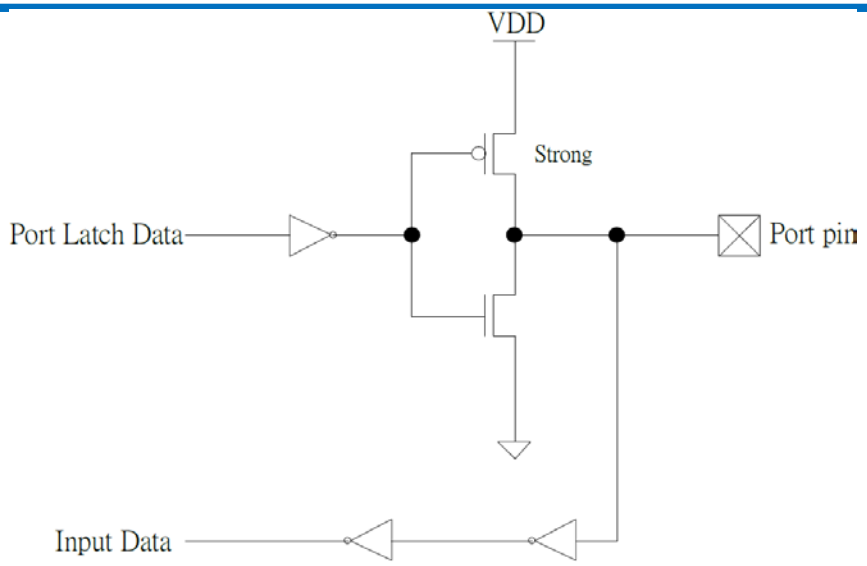


Figure 2.4.11.16 Push-pull mode (Output)

2.4.11.17 Open drain mode

Set GPIOxPMS register to 0x2 the Pin (n) in Open-Drain mode and the I/O pin supports digital output function but it only with sink current capability, an additional pull-up resister in need for driving high state.

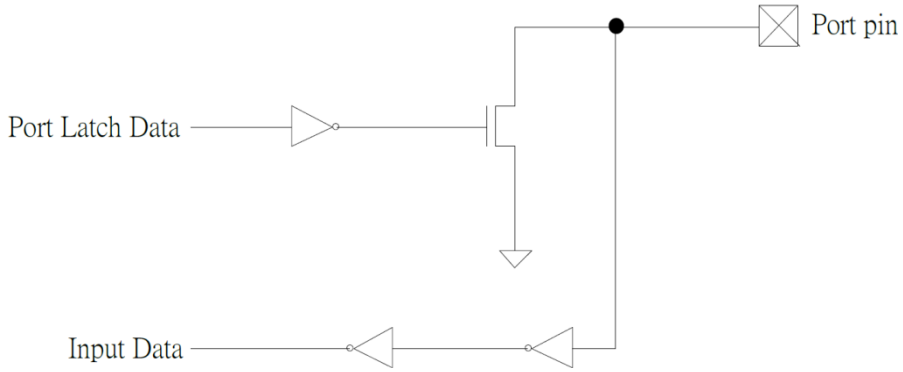


Figure 2.4.11.17 Open drain mode

2.4.11.18 Input only mode (high-impedance)

Set GPIOxPMS register to 0x3 the Pin(n) in Input only mode and I/O pin is in high impedance without output drive capability.

2.4.12 Nested Vectored Interrupt Controller (NVIC Base address = 0xE000_E000)

This section describes the NVIC and the registers it uses. The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-32.
- A programmable priority level of 0-192 in steps of 64 for each interrupt. A higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling. The hardware implementation of the NVIC registers is:

Name	Offset	Access	Description	Reset value
ISER	0x100	R/W	Interrupt Set-enable Register.	0x00000000
ICER	0x180	R/W	Interrupt Clear-enable Register.	0x00000000
ISPR	0x200	R/W	Interrupt Set-pending Register.	0x00000000
ICPR	0x280	R/W	Interrupt Clear-pending Register.	0x00000000
IPR0	0x400	R/W	IRQ0 ~ IRQ3 Interrupt Priority Register.	0x00000000
IPR1	0x404	R/W	IRQ4 ~ IRQ7 Interrupt Priority Register.	0x00000000
IPR2	0x408	R/W	IRQ8 ~ IRQ11 Interrupt Priority Register.	0x00000000
IPR3	0x40C	R/W	IRQ12 ~ IRQ15 Interrupt Priority Register.	0x00000000
IPR4	0x410	R/W	IRQ16 ~ IRQ19 Interrupt Priority Register.	0x00000000
IPR5	0x414	R/W	IRQ20 ~ IRQ23 Interrupt Priority Register.	0x00000000
IPR6	0x418	R/W	IRQ24 ~ IRQ27 Interrupt Priority Register.	0x00000000
IPR7	0x41C	R/W	IRQ28 ~ IRQ31 Interrupt Priority Register.	0x00000000

Table 2.4.12 Register Overview: Nested Vectored Interrupt Controller (NVIC)

2.4.12.1 Accessing the Cortex-M0 NVIC registers using CMSIS

CMSIS functions enable software portability between different Cortex-M profile processors. To access the NVIC registers when using CMSIS, use the following functions:

CMSIS function	Description
void NVIC_EnableIRQ(IRQn_Type IRQn)	Enables an interrupt or exception.
void NVIC_DisableIRQ(IRQn_Type IRQn)	Disables an interrupt or exception.
void NVIC_SetPendingIRQ(IRQn_Type IRQn)	Sets the pending status of interrupt or exception to 1.
void NVIC_ClearPendingIRQ(IRQn_Type IRQn)	Clears the pending status of interrupt or exception to 0.

uint32_t NVIC_GetPendingIRQ(IRQn_Type IRQn)	Reads the pending status of interrupt or exception. This function returns non-zero value if the pending status is set to 1.
void NVIC_SetPriority(IRQn_Type IRQn, uint32_t priority)	Sets the priority of an interrupt or exception with configurable priority level to 1.
uint32_t NVIC_GetPriority(IRQn_Type IRQn)	Reads the priority of an interrupt or exception with configurable priority level. This function returns the current priority level.

Table 2.4.12.1 Accessing the Cortex-M0 NVIC registers using CMSIS

The input parameter IRQn is the IRQ number.

2.4.12.2 Interrupt Set-enable Register (ISER)

The ISER enables interrupts, and shows the interrupts that are enabled.

Bit	Symbol	Description	Reset value
31:0	SETENA	Interrupt set-enable bits. Write: 0 = no effect 1 = enable interrupt. Read: 0 = interrupt disabled 1 = interrupt enabled.	0x00000000

Table 2.4.12.2 Interrupt Set-enable Register (ISER)

If a pending interrupt is enabled, the NVIC activates the interrupt based on its priority.
If an interrupt is not enabled, asserting its interrupt signal changes the interrupt state to pending, but the NVIC never activates the interrupt, regardless of its priority.

2.4.12.3 Interrupt Clear-enable Register (ICER)

The ICER disables interrupts, and shows the interrupts that are enabled.

Bit	Symbol	Description	Reset value

31:0	CLRENA	Interrupt clear-enable bits. Write: 0 = no effect 1 = disable interrupt. Read: 0 = interrupt disabled 1 = interrupt enabled.	0x00000000

Table 2.4.12.3 Interrupt Clear-enable Register (ICER)

2.4.12.4 Interrupt Set-pending Register (ISPR)

The ISPR forces interrupts into the pending state, and shows the interrupts that are pending.

Bit	Symbol	Description	Reset value
31:0	SETPEND	Interrupt set-pending bits. Write: 0 = no effect 1 = changes interrupt state to pending. Read: 0 = interrupt is not pending 1 = interrupt is pending.	0x00000000

Table 2.4.12.4 Interrupt Set-pending Register (ISPR)

Note:

Writing 1 to the ISPR bit corresponding to:

- an interrupt that is pending has no effect
- a disabled interrupt sets the state of that interrupt to pending.

2.4.12.5 Interrupt Clear-pending Register (ICPR)

The ICPR removes the pending state from interrupts, and shows the interrupts that are pending.

Bit	Symbol	Description	Reset value
31:0	CLRPEND	Interrupt clear-pending bits. Write: 0 = no effect 1 = removes pending state an interrupt. Read: 0 = interrupt is not pending 1 = interrupt is pending.	0x00000000

Table 2.4.12.5 Interrupt Clear-pending Register (ICPR)

Note:

Writing 1 to an ICPR bit does not affect the active state of the corresponding interrupt.

2.4.12.6 Interrupt Priority Registers (IPR0~7)

The interrupt priority registers provide an 8-bit priority field for each interrupt, and each register holds four priority fields. This means the number of registers is implementation-defined, and corresponds to the number of implemented interrupts. These registers are only word-accessible. For an implementation that supports 32 interrupts the registers are IPR0-IPR7.

2.4.12.6.1 IRQ0 ~ IRQ3 Interrupt Priority Register (IPR0)

Bit	Symbol	Description	Reset value
31:30	PRI_3	The lower the value, the greater the priority of the corresponding interrupt.	0x0
29:24	-	Reserved.	-
23:22	PRI_2	The lower the value, the greater the priority of the corresponding interrupt.	0x0
21:16	-	Reserved.	-
15:14	PRI_1	The lower the value, the greater the priority of the corresponding interrupt.	0x0
13:8	-	Reserved.	-
7:6	PRI_0	The lower the value, the greater the priority of the corresponding interrupt.	0x0
5:0	-	Reserved.	-

Table 2.4.12.6.1 IRQ0 ~ IRQ3 Interrupt Priority Register (IPR0)

2.4.12.6.2 IRQ4 ~ IRQ7 Interrupt Priority Register (IPR1)

Bit	Symbol	Description	Reset value
31:30	PRI_7	The lower the value, the greater the priority of the corresponding interrupt.	0x0
29:24	-	Reserved, should not write value to the none defined bits	-

23:22	PRI_6	The lower the value, the greater the priority of the corresponding interrupt.	0x0
21:16	-	Reserved, should not write value to the none defined bits	-
15:14	PRI_5	The lower the value, the greater the priority of the corresponding interrupt.	0x0
13:8	-	Reserved, should not write value to the none defined bits	-
7:6	PRI_4	The lower the value, the greater the priority of the corresponding interrupt.	0x0
5:0	-	Reserved, should not write value to the none defined bits	-

Table 2.4.12.6.2 IRQ4 ~ IRQ7 Interrupt Priority Register (IPR1)

2.4.12.6.3 RQ8 ~ IRQ11 Interrupt Priority Register (IPR2)

Bit	Symbol	Description	Reset value
31:30	PRI_11	The lower the value, the greater the priority of the corresponding interrupt.	0x0
29:24	-	Reserved, should not write value to the none defined bits	-
23:22	PRI_10	The lower the value, the greater the priority of the corresponding interrupt.	0x0
21:16	-	Reserved, should not write value to the none defined bits	-
15:14	PRI_9	The lower the value, the greater the priority of the corresponding interrupt.	0x0
13:8	-	Reserved, should not write value to the none defined bits	-
7:6	PRI_8	The lower the value, the greater the priority of the corresponding interrupt.	0x0
5:0	-	Reserved, should not write value to the none defined bits	-

Table 2.4.12.6.3 IRQ8 ~ IRQ11 Interrupt Priority Register (IPR2)

2.4.12.6.4 IRQ12 ~ IRQ15 Interrupt Priority Register (IPR3)

Bit	Symbol	Description	Reset value
31:30	PRI_15	The lower the value, the greater the priority of the corresponding interrupt.	0x0
29:24	-	Reserved, should not write value to the none defined bits	-
23:22	PRI_14	The lower the value, the greater the priority of the corresponding interrupt.	0x0

21:16	-	Reserved, should not write value to the none defined bits	-
15:14	PRI_13	The lower the value, the greater the priority of the corresponding interrupt.	0x0
13:8	-	Reserved, should not write value to the none defined bits	-
7:6	PRI_12	The lower the value, the greater the priority of the corresponding interrupt.	0x0
5:0	-	Reserved, should not write value to the none defined bits	-

Table 2.4.12.6.4 IRQ12 ~ IRQ15 Interrupt Priority Register (IPR3)

2.4.12.6.5 IRQ16 ~ IRQ19 Interrupt Priority Register (IPR4)

Bit	Symbol	Description	Reset value
31:30	PRI_19	The lower the value, the greater the priority of the corresponding interrupt.	0x0
29:24	-	Reserved, should not write value to the none defined bits	-
23:22	PRI_18	The lower the value, the greater the priority of the corresponding interrupt.	0x0
21:16	-	Reserved, should not write value to the none defined bits	-
15:14	PRI_17	The lower the value, the greater the priority of the corresponding interrupt.	0x0
13:8	-	Reserved, should not write value to the none defined bits	-
7:6	PRI_16	The lower the value, the greater the priority of the corresponding interrupt.	0x0
5:0	-	Reserved, should not write value to the none defined bits	-

Table 2.4.12.6.5 IRQ16 ~ IRQ19 Interrupt Priority Register (IPR4)

2.4.12.6.6 IRQ20 ~ IRQ23 Interrupt Priority Register (IPR5)

Bit	Symbol	Description	Reset value
31:30	PRI_23	The lower the value, the greater the priority of the corresponding interrupt.	0x0
29:24	-	Reserved, should not write value to the none defined bits	-
23:22	PRI_22	The lower the value, the greater the priority of the corresponding interrupt.	0x0
21:16	-	Reserved, should not write value to the none defined bits	-

15:14	PRI_21	The lower the value, the greater the priority of the corresponding interrupt.	0x0
13:8	-	Reserved, should not write value to the none defined bits	-
7:6	PRI_20	The lower the value, the greater the priority of the corresponding interrupt.	0x0
5:0	-	Reserved, should not write value to the none defined bits	-

Table 2.4.12.6.6 IRQ20 ~ IRQ23 Interrupt Priority Register (IPR5)

2.4.12.6.7 IRQ24 ~ IRQ27 Interrupt Priority Register (IPR6)

Bit	Symbol	Description	Reset value
31:30	PRI_27	The lower the value, the greater the priority of the corresponding interrupts.	0x0
29:24	-	Reserved, should not write value to the none defined bits	-
23:22	PRI_26	The lower the value, the greater the priority of the corresponding interrupts.	0x0
21:16	-	Reserved, should not write value to the none defined bits	-
15:14	PRI_25	The lower the value, the greater the priority of the corresponding interrupts.	0x0
13:8	-	Reserved, should not write value to the none defined bits	-
7:6	PRI_24	The lower the value, the greater the priority of the corresponding interrupts.	0x0
5:0	-	Reserved, should not write value to the none defined bits	-

Table 2.4.12.6.7 IRQ24 ~ IRQ27 Interrupt Priority Register (IPR6)

2.4.12.6.8 IRQ28 ~ IRQ31 Interrupt Priority Register (IPR7)

Bit	Symbol	Description	Reset value
31:30	PRI_31	The lower the value, the greater the priority of the corresponding interrupt.	0x0
29:24	-	Reserved, should not write value to the none defined bits	-
23:22	PRI_30	The lower the value, the greater the priority of the corresponding interrupt.	0x0
21:16	-	Reserved, should not write value to the none defined bits	-
15:14	PRI_29	The lower the value, the greater the priority of the corresponding interrupt.	0x0

13:8	-	Reserved, should not write value to the none defined bits	-
7:6	PRI_28	The lower the value, the greater the priority of the corresponding interrupt.	0x0
5:0	-	Reserved, should not write value to the none defined bits	-

Table 2.4.12.6.8 IRQ28 ~ IRQ31 Interrupt Priority Register (IPR7)

2.4.12.7 NVIC usage hints and tips

Ensure software uses correctly aligned register accesses. The processor does not support unaligned accesses to NVIC registers.

An interrupt can enter pending state even if it is disabled. Disabling an interrupt only prevents the processor from taking that interrupt.

NVIC programming hints

Software uses the CPSIE i and CPSID i instructions to enable and disable interrupts. The CMSIS provides the following intrinsic functions for these instructions:

void disable_irq(void) // Disable Interrupts

void enable_irq(void) // Enable Interrupts

In addition, the CMSIS provides a number of functions for NVIC control, including:

CMSIS function	Description
void NVIC_EnableIRQ(IRQn_t IRQn)	Enable IRQn
void NVIC_DisableIRQ(IRQn_t IRQn)	Disable IRQn
uint32_t NVIC_GetPendingIRQ (IRQn_t IRQn)	Return true (1) if IRQn is pending
void NVIC_SetPendingIRQ (IRQn_t IRQn)	Set IRQn pending
void NVIC_ClearPendingIRQ (IRQn_t IRQn)	Clear IRQn pending status
void NVIC_SetPriority (IRQn_t IRQn, uint32_t priority)	Set priority for IRQn
uint32_t NVIC_GetPriority (IRQn_t IRQn)	Read priority of IRQn
void NVIC_SystemReset (void)	Reset the system

Table 2.4.12.7 NVIC programming hints

The input parameter IRQn is the IRQ number.

2.4.12.8 Interrupt sources

Exception Number	IRQ Number	Vector Address	Function	Flag(s)
1-15	-	0x00-0x3C	System exceptions	
16	0	0x40	GPIO0 (GP0)	GPIO P0[7:0] interrupt
17	1	0x44	GPIO1 (GP1)	GPIO P1[7:0] interrupt
18	2	0x48	GPIO2 (GP2)	GPIO P2[7:0] interrupt
19	3	0x4C	GPIO3 (GP3)	GPIO P3[0] interrupt
20	4	0x50	-	-
21	5	0x54	Capture/PWM (PWM)	Capture interrupt PWM compare interrupt Count overflow
22	6	0x58	ADC	A/D Converter end of conversion
23	7	0x5C	-	-
24	8	0x60	-	-
25	9	0x64	-	-
26	10	0x68	-	-
27	11	0x6C	-	-
28	12	0x70	-	-
29	13	0x74	-	-
30	14	0x78	-	-
31	15	0x7C	UART0	Rx Line Status (RLS) Transmit Holding Register Empty (THRE) Rx Data Available (RDA) Character Time-out Indicator (CTI)
32	16	0x80	UART1	Rx Line Status (RLS) Transmit Holding Register Empty (THRE) Rx Data Available (RDA) Character Time-out Indicator (CTI)
33	17	0x84	UART2	Rx Line Status (RLS) Transmit Holding Register Empty (THRE) Rx Data Available (RDA)

				Character Time-out Indicator (CTI)
34	18	0x88	-	-
35	19	0x8C	Timer0	Timer0 Overflow
36	20	0x90	Timer1	Timer1 Overflow
37	21	0x94	-	-
38	22	0x98	-	-
39	23	0x9C	WDT	Watchdog Timer interrupt
40	24	0xA0	I2C0	SI (state change)
41	25	0xA4	-	-
42	26	0xA8	SSP0	Tx FIFO half empty Rx FIFO half full Rx Timeout Rx Overrun
43	27	0xAC	-	-
44	28	0xB0	-	-
45	29	0xB4	-	-
46	30	0xB8	-	-
47	31	0xBC	-	-

Table 2.4.12.8 Interrupt sources

2.4.13 System Control Block (SCB Base address = 0xE000_E000)

The SCB provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions.

Name	Offset	Access	Description	Reset value
CPUID	0xD00	RO	CPUID Register.	0x410CC200
ICSR	0xD04	R/W	Interrupt Control and State Register	0x00000000
AIRCR	0xD0C	R/W	Application Interrupt and Reset Control Register	0xFA050000
SCR	0xD10	R/W	System Control Register	0x00000000
CCR	0xD14	RO	Configuration and Control Register	0x00000208
SHPR2	0xD1C	R/W	System Handler Priority Register 2	0x00000000
SHPR3	0xD20	R/W	System Handler Priority Register 3	0x00000000

Table 2.4.13 System Control Block (SCB)

2.4.13.1 The CMSIS mapping of the Cortex-M0 SCB registers

To improve software efficiency, the CMSIS simplifies the SCB register presentation. In the CMSIS, the array SHP[1] corresponds to the registers SHPR2-SHPR3.

2.4.13.2 CPUID Register

The CPUID register contains the processor part number, version, and implementation information. The reset value depends on the variant and patch values of the implemented device.

Bit	Symbol	Description	Reset value
31:24	Implementer	Implementer code: 0x41 corresponds to ARM	0x41
23:20	Variant	Variant number, the r value in the rnpn product revision identifier: 0x0 corresponds to revision 0	0x0
19:16	Constant	Constant that defines the architecture of the processor:, reads as 0xC corresponds to ARMv6-M architecture	0xC
15:4	Partno	Part number of the processor: 0xC20 corresponds to Cortex-M0	0xC20
3:0	Revision	Revision number, the p value in the rnpn product revision identifier: 0x0 corresponds to patch 0	0x0

Table 2.4.14.2 CPUID Register

2.4.13.3 Interrupt Control and State Register (ICSR)

The ICSR:

- provides:
  - a set-pending bit for the NMI exception
  - set-pending and clear-pending bits for the PendSV and SysTick exceptions
- indicates:
  - the exception number of the exception being processed
  - whether there are preempted active exceptions
  - the exception number of the highest priority pending exception
  - whether any interrupts are pending.

Bit	Symbol	Description	Reset value
31	NMIPENDSET	NMI set-pending bit. Write: 0 = no effect 1 = changes NMI exception state to pending. Read: 0 = NMI exception is not pending 1 = NMI exception is pending. Because NMI is the highest-priority exception, normally the processor enters the NMI exception handler as soon as it detects a write of 1 to this bit. Entering the handler then clears this bit to 0. This means a read of this bit by the NMI exception handler returns 1 only if the NMI signal is reasserted while the processor is executing that handler.	0
30:29	-	Reserved.	-
28	PENDSVSET	PendSV set-pending bit. Write: 0 = no effect 1 = changes PendSV exception state to pending. Read: 0 = PendSV exception is not pending 1 = PendSV exception is pending. Writing 1 to this bit is the only way to set the PendSV exception state to pending.	0
27	PENDSVCLR	PendSV clear-pending bit. Write:	-

		0 = no effect 1 = removes the pending state from the PendSV exception. This bit is WO. On a register read its value is Unknown.	
26	PENDSTSET	SysTick exception set-pending bit. Write: 0 = no effect 1 = changes SysTick exception state to pending. Read: 0 = SysTick exception is not pending 1 = SysTick exception is pending.	0
25	PENDSTCLR	SysTick exception clear-pending bit. Write: 0 = no effect 1 = removes the pending state from the SysTick exception. This bit is WO. On a register read its value is Unknown.	-
24:23	-	Reserved.	-
22	ISRPENDING	Interrupt pending flag, excluding NMI and Faults: 0 = interrupt not pending 1 = interrupt pending. This bit is RO.	0
21:18	-	Reserved.	-
17:12	VECTPENDING	Indicates the exception number of the highest priority pending enabled exception: 0 = no pending exceptions Nonzero = the exception number of the highest priority pending enabled exception. Read only.	0x00
11:6	-	Reserved.	-
5:0	VECTACTIVE	Contains the active exception number: 0 = Thread mode Nonzero = The exception number of the currently active exception. Note: Subtract 16 from this value to obtain the CMSIS IRQ number that identifies the corresponding bit in the Interrupt Clear-Enable, Set-Enable, Clear-Pending, Set-pending, and Priority Register. This is the same value as IPSR bits[5:0]. Read only.	0x00

Table 2.4.13.3 Interrupt Control and State Register (ICSR)

When you write to the ICSR, the effect is Unpredictable if you:

- write 1 to the PENDSVSET bit and write 1 to the PENDSVCLR bit
- write 1 to the PENDSTSET bit and write 1 to the PENDSTCLR bit.

2.4.13.4 Application Interrupt and Reset Control Register (AIRCR)

The AIRCR provides endian status for data accesses and reset control of the system.
To write to this register, you must write 0x05FA to the VECTKEY field, otherwise the processor ignores the write.

Bit	Symbol	Description	Reset value
31:16	Read: Reserved Write: VECTKEY	Register key: Reads as Unknown On writes, write 0x05FA to VECTKEY, otherwise the write is ignored.	0xFA05
15	ENDIANESS	Data endianness implemented: 0 = Little-endian 1 = Big-endian. This bit is RO.	0
14:3	-	Reserved.	-
2	SYSRESETREQ	System reset request: 0 = no effect 1 = requests a system level reset. This bit reads as 0.	0
1	VECTCLRACTIVE	Reserved for debug use. This bit reads as 0. When writing to the register you must write 0 to this bit, otherwise behavior is Unpredictable.	0
0	-	Reserved.	-

Table 2.4.13.4 Application Interrupt and Reset Control Register (AIRCR)

2.4.13.5 System Control Register (SCR)

The SCR controls features of entry to and exit from low power state.

Bit	Symbol	Description	Reset value
31:5	-	Reserved.	-

4	SEVONPEND	Send Event on Pending bit: 0 = only enabled interrupts or events can wake-up the processor, disabled interrupts are excluded 1 = enabled events and all interrupts, including disabled interrupts, can wake-up the processor. When an event or interrupt enters pending state, the event	0
3	-	Reserved.	-
2	SLEEPDEEP	Controls whether the processor uses sleep or deep sleep as its low power mode: 0 = sleep 1 = deep sleep. Note: This bit is always zero.	0
1	SLEEPONEXIT	Indicates sleep-on-exit when returning from Handler mode to Thread mode: 0 = do not sleep when returning to Thread mode. 1 = enter sleep, or deep sleep, on return from an ISR to Thread mode. Setting this bit to 1 enables an interrupt driven application to	0
0	-	Reserved.	-

Table 2.4.13.5 System Control Register (SCR)

2.4.13.6 Configuration and Control Register (CCR)

The CCR is a read-only register and indicates some aspects of the behavior of the Cortex-M0 processor.

Bit	Symbol	Description	Reset value
31:10	-	Reserved.	-

9	STKALIGN	Always reads as one, indicates 8-byte stack alignment on exception entry. On exception entry, the processor uses bit[9] of the stacked PSR to indicate the stack alignment. On return from the exception it uses this stacked bit to restore the correct stack alignment.	1
8:4	-	Reserved.	-
3	UNALIGN_TRP	Always reads as one, indicates that all unaligned accesses generate a HardFault.	1
2:0	-	Reserved.	-

Table 2.4.13.6 Configuration and Control Register (CCR)

2.4.13.7 System Handler Priority Registers

The SHPR2-SHPR3 registers set the priority level, 0 to 192, of the exception handlers that have configurable priority.

SHPR2-SHPR3 are word accessible.

To access to the system exception priority level using CMSIS, use the following CMSIS functions:

- uint32_t NVIC_GetPriority(IRQn_Type IRQn)

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- void NVIC_SetPriority(IRQn_Type IRQn, uint32_t priority)

The input parameter IRQn is the IRQ number.

The system fault handlers, and the priority field and register for each handler are:

Handler	Field	Register description
SVCall	PRI_11	System Handler Priority Register 2
PendSV	PRI_14	System Handler Priority Register 3
SysTick	PRI_15	

Table 2.4.13.7 System Handler Priority

Registers Each PRI_N field is 8 bits wide, but the processor implements only bits[7:6] of each field, and bits[5:0] read as zero and ignore writes.

2.4.13.8 System Handler Priority Register 2 (SHPR2)

Bit	Symbol	Description	Reset value
31:24	PRI_11	Priority of system handler 11, SVCall	0x00
23:0	-	Reserved.	-

Table 2.4.13.8 System Handler Priority Register 2 (SHPR2)

2.4.13.9 System Handler Priority Register 3 (SHPR3)

Bit	Symbol	Description	Reset value
31:24	PRI_15	Priority of system handler 15, SysTick exception	0x00
23:16	PRI_14	Priority of system handler 14, PendSV	0x00
15:0	-	Reserved.	-

Table 2.4.13.9 System Handler Priority Register 3 (SHPR3)

2.4.13.10 SCB usage hints and tips

Ensure software uses aligned 32-bit word size transactions to access all the SCB registers.

2.4.14 System timer (SysTick Base address = 0xE000_E000)

If implemented, when enabled, the timer counts down from the reload value to zero, reloads (wraps to) the value in the SYST_RVR on the next clock cycle, then decrements on subsequent clock cycles. Writing a value of zero to the SYST_RVR disables the counter on the next wrap. When the counter transitions to zero, the COUNTFLAG status bit is set to 1. Reading SYST_CSR clears the COUNTFLAG bit to 0.

Writing to the SYST_CVR clears the register and the COUNTFLAG status bit to 0. The write does not trigger the SysTick exception logic. Reading the register returns its value at the time it is accessed.

Note:

When the processor is halted for debugging the counter does not decrement.

Name	Offset	Access	Description	Reset value
SysTickCTRL	0x010	R/W	SysTick Control and Status Register.	0x00000000
SysTickLOAD	0x014	R/W	SysTick Reload Value Register.	-
SysTickVAL	0x018	R/W	SysTick Current Value Register.	-
SysTickCALIB	0x01C	RO	SysTick Calibration Value Register.	0x00000004

Table 2.4.14 Register Overview: System timer (SysTick)

2.4.14.1 SysTick Control and Status Register (SysTickCTRL)

The SYST_CSR enables the SysTick features. The register resets to 0x00000000, or 0x00000002 if your device does not implement a reference clock.

Bit	Symbol	Description	Reset value

31:17	-	Reserved.	-
16	COUNTFLAG	Returns 1 if timer counted to 0 since the last read of this register.	0
15:3	-	Reserved.	-
2	CLKSOURCE	Selects the SysTick timer clock source: 0 = external reference clock. 1 = processor clock.	0
1	INT	Enables SysTick exception request: 0 = counting down to zero does not assert the SysTick exception request.	0
0	EN	Enables the counter: 0 = counter disabled. 1 = counter enabled.	0

Table 2.4.14.1 SysTick Control and Status Register (SysTickCTRL)

2.4.14.2 SysTick Reload Value Register (SysTickLOAD)

The SYST_RVR specifies the start value to load into the SYST_CVR.

Bit	Symbol	Description	Reset value
31:24	-	Reserved.	-
23:0	RELOAD	Value to load into the SYST_CVR when the counter is enabled and when it reaches 0.	-

Table 2.4.14.2 SysTick Reload Value Register (SysTickLOAD

Calculating the RELOAD value

The RELOAD value can be any value in the range 0x00000001-0x00FFFFFF. You can program a value of 0, but this has no effect because the SysTick exception request and COUNTFLAG are activated when counting from 1 to 0.

To generate a multi-shot timer with a period of N processor clock cycles, use a RELOAD value of N-1. For example, if the SysTick interrupt is required every 100 clock pulses, set RELOAD to 99.

2.4.14.3 SysTick Current Value Register (SysTickVAL)

The SYST_CVR contains the current value of the SysTick counter.

Bit	Symbol	Description	Reset value
31:24	-	Reserved.	-

23:0	CURRENT	Reads return the current value of the SysTick counter. A write of any value clears the field to 0, and also clears the SYST_CSR.COUNTFLAG bit to 0.	-

Table 2.4.14.3 SysTick Current Value Register (SysTickVAL)

2.4.14.4 SysTick Calibration Value Register (SysTickCALIB)

The SYST_CALIB register indicates the SysTick calibration properties. The reset value of this register is implementation-defined. See the documentation supplied by your device vendor for more information about the meaning of the SYST_CALIB field values.

Bit	Symbol	Description	Reset value
31	NOREF	Reads as one. Indicates that no separate reference clock is provided.	0
30	SKEW	Reads as one. Calibration value for the 10ms inexact timing is not known because TENMS is not known. This can affect the suitability of SysTick as a software real time clock.	-
29:24	-	Reserved.	-
23:0	TENMS	Reads as zero. Indicates calibration value is not known.	0x000004

Table 2.4.14.4 SysTick Calibration Value Register (SysTickCALIB)

2.4.15 User Configuration (Base address = 0x1000_0000)

Name	Offset	Access	Description	Default value
MCUCON	0x000	R/W	MCU Configuration Register.	0xFF
IOMUX	0x004	R/W	IO Function Configuration Register.	0xFF

Table 2.4.15 Register Overview: User Configurat

2.4.15.1 MCU Configuration Register (MCUCON)

Bit	Symbol	Description	Reset value
31:9	Reserved	Reserved.	-
8	XTALSEL	XTAL pad select 1: XTAL 1~25MHz is select 0: XTAL 32.768KHz is select	1
7:5	Reserved	Reserved.	-
4	SWDP	SWD Protect (Hardware auto unprotected, when run FMCFUNC command 0x6 or 0x7) 1: SWD Unprotected 0: SWD Protected	1
3	FMC	ISP Mapping Enable 1: Disable (Boot from main code) 0: Enable (Boot from ISP code)	1
2:0	Reserved	Reserved.	-

Table 2.4.15.1 MCU Configuration Register (MCUCON)

2.4.15.2 IO function Configuration Register (IOMUX)

Bit	Symbol	Description	Reset value
31:10	-	Reserved.	-
9	XTALPORT	XTAL pin location 0: P1.0/P1.1 assign to GPIO function. 1: P1.0/P1.1 assign to XTAL function.	-
8	RESETPORT	External reset pin location 0: Enable external reset function. When external reset function enable, the reset pin will assign to P14 and P14 GPIO function MUX will disable. 1: Disable external reset function.	-

7:4	SWCLK_PORT	SWDLK pin location 0xF : SWCLK pin assign to P13 and P13 GPIO function select disable. 0xE : SWCLK pin assign to P20 and P20 GPIO function select disable. 0xD : SWCLK pin assign to P01 and P01 GPIO function select disable. 0xC : SWCLK pin assign to P26 and P26 GPIO function select disable. 0xB : SWCLK pin assign to P23 and P23 GPIO function select disable. 0xA : SWCLK pin assign to P03 and P03 GPIO function select disable. 0x9 : SWCLK pin assign to P05 and P05 GPIO function select disable. 0x8 : SWCLK pin assign to P16 and P16 GPIO function select disable. 0x7 : SWCLK pin assign to P07 and P07 GPIO function select disable. 0x6 : SWCLK pin assign to P30 and P30 GPIO function select disable. 0x5 : SWCLK pin assign to P22 and P22 GPIO function select disable. Others : SWCLK function pin disable.	-

3:0	SWDIO_PORT	SWDIO pin location 0xF : SWDIO pin assign to P12 and P12 GPIO function select disable. 0xE : SWDIO pin assign to P00 and P00 GPIO function select disable. 0xD : SWDIO pin assign to P15 and P15 GPIO function select disable. 0xC : SWDIO pin assign to P25 and P25 GPIO function select disable. 0xB : SWDIO pin assign to P24 and P24 GPIO function select disable. 0xA : SWDIO pin assign to P02 and P02 GPIO function select disable. 0x9 : SWDIO pin assign to P04 and P04 GPIO function select disable. 0x8 : SWDIO pin assign to P17 and P17 GPIO function select disable. 0x7 : SWDIO pin assign to P06 and P06 GPIO function select disable. 0x6 : SWDIO pin assign to P27 and P27 GPIO function select disable. 0x5 : SWDIO pin assign to P21 and P21 GPIO function select disable. Others : Disable SWDIO pin function.	

Table 2.4.15.2 IO function Configuration Register (IOMUX

3 RF

3.1 Introduction

The HS6207 uses the same 2.4 GHz GFSK RF transceiver with embedded protocol engine. The RF transceiver is designed for operation in the world wide ISM frequency band at 2.400–2.4835 GHz and is very well suited for ultra-low power wireless applications.

The RF transceiver module is configured and operated through the RF transceiver map. This register map is accessed by the MCU through a dedicated on-chip Serial Peripheral interface (SPI) and is available in all power modes of the RF transceiver module. The embedded protocol engine enables data packet communication and supports various modes from manual operation to advanced autonomous protocol operation. Data FIFOs in the RF transceiver module ensure a smooth data flow between the RF transceiver module and the HS6207 MCU.

The rest of this chapter is written in the context of the RF transceiver module as the core and the rest of the HS6207 as external circuitry to this module.

3.1.1 Features

Features of the RF include:

- Radio:
  - Worldwide 2.4GHz ISM band operation
  - 126 RF channels
  - Common RX and TX interface
  - GFSK modulation
  - 500kbps, 1 and 2Mbps air data rate
  - 1MHz non-overlapping channel spacing at 1Mbps
  - 2MHz non-overlapping channel spacing at 2Mbps
- Transmitter:
  - Programmable output power:8 , 5, 4, 0, -6, -12 ,-16 or -43dBm。
- Receiver:
  - Fast AGC for improved dynamic range
  - Integrated channel filters
  - -83dBm sensitivity at 2Mbps
  - -89dBm sensitivity at 1Mbps
  - -89dBm sensitivity at 500kbps
- RF Synthesizer:
  - Fully integrated synthesizer
  - No external loop filer, VCO varactor diode or resonator
  - Accepts low cost ±60ppm 16MHz crystal
- Protocol engine:
  - 1 to 32 bytes dynamic payload length
  - Automatic packet handling
  - Auto packet transaction handling
  - 6 data pipe for 1:6 star networks
- Power Management:
  - Integrated voltage regulator
  - 1.8 to 3.6V supply range
  - Idle modes with fast start-up times for advanced power management
  - 30μA Standby-I mode,4Ua power down mode
  - Max 2ms start-up from power down mode
  - Max 210us start-up from standby-I mode
- Host Interface:
  - 4-pin hardware SPI
  - Max 10Mbps
  - 3 separate 32 bytes TX and RX FIFOs
  - 5V tolerant IO

3.1.2 **Block**

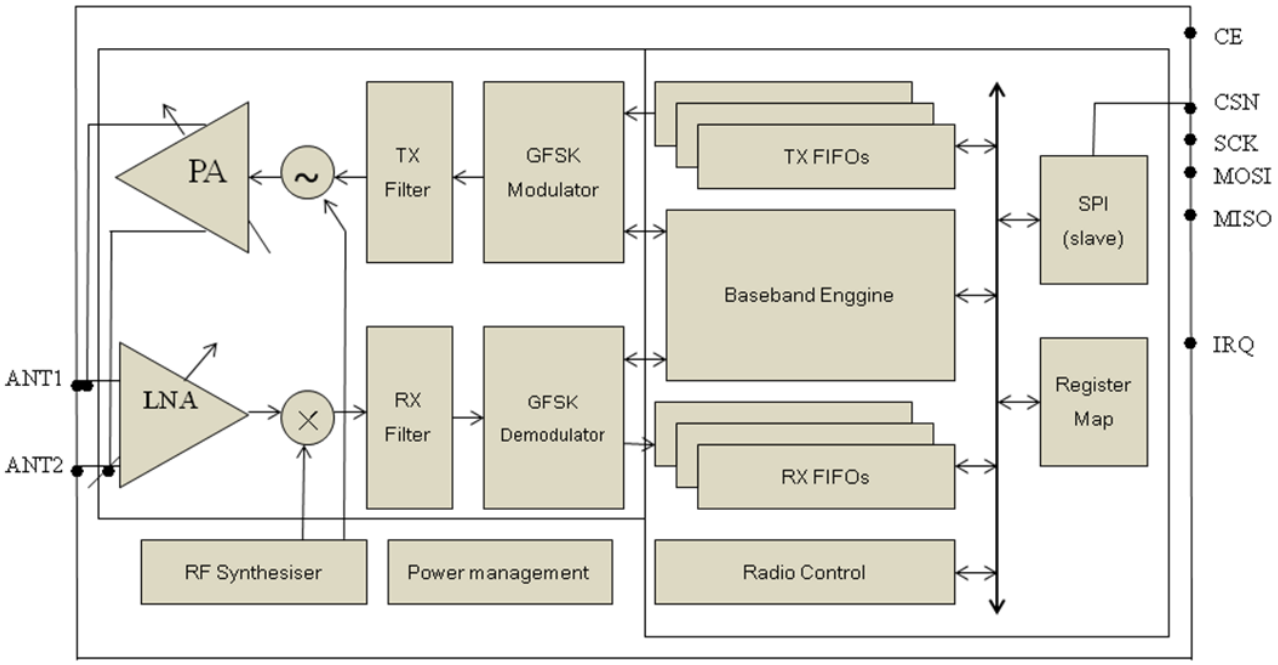


Figure3.1.2 RF block diagram

3.2 Radio Control

This chapter describes the RF radio transceiver's operating modes and the parameters used to control the radio.

The RF has a built-in state machine that controls the transitions between the chip's operating modes. The state machine takes input from user defined register values and internal signals.

3.2.1 Operational Modes

You can configure the RF in power down, standby, RX or TX mode. This section describes these modes in detail.

3.2.1.1 State diagram

There are three types of distinct states highlighted in the state diagram:

- Recommended operating mode: is a recommended state used during normal operation.
- Possible operating mode: is a possible operating state, but is not used during normal operation.
- Transition state: is a time limited state used during start up of the oscillator and settling of the PLL.

When the VDD reaches 1.8V or higher RF enters the Power on reset state where it remains in reset until entering the Power Down mode.

3.2.1.2 Power Down Mode

In power down mode, the RF is disabled using minimize average current consumption. All register values available are maintained and the SPI is kept active, enabling change of configuration and the uploading/down-loading of data registers. Power down mode is entered by setting the PWR_UP bit in the CONFIG register low.

3.2.1.3 Standby Modes

3.2.1.3.1 Standby-I mode

By setting the PWR_UP bit in the CONFIG register to 1, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start up times. In this mode only part of the crystal oscillator is active. Change to active modes only happens if CE is set high and when CE is set low, the RF returns to standby-I mode from both the TX and RX modes.

3.2.1.3.2 Standby-II mode

In standby-II mode extra clock buffers are active and more current is used compared to standby-I mode. The RF enters standby-II mode if CE is held high on a PTX device with an empty TX FIFO. If a new packet is uploaded to the TX FIFO, the PLL immediately starts and the packet is transmitted after the normal PLL settling delay (210µs). Register values are maintained and the SPI can be activated during both standby modes.

Notice: From Standby-I mode to standby-II mode CE more than 20us

3.2.1.4 RX mode

The RX mode is an active mode where the RF radio is used as a receiver. To enter this mode, the chip must have the PWR_UP bit, PRIM_RX bit and the CE pin set high.

In RX mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the baseband protocol engine. The baseband protocol engine constantly searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFOs. If the RX FIFOs are full, the received packet is discarded.

The chip remains in RX mode until the MCU configures it to standby-I mode or power down mode. However, if the automatic protocol features in the baseband protocol engine are enabled, the chip can enter other modes in order to execute the protocol.

In RX mode a Received Power Detector (RPD) signal is available. The RPD register is a signed number which corresponds to different level of received power in dBm. The highest bit of RPD is sign bit. The range of the received power is -100 ~ +10dBm. The RPD has about +/-5dBm deviation from the real level.

3.2.1.5 TX mode

The TX mode is an active mode for transmitting packets. To enter this mode, the chip must have the PWR_UP bit set high, PRIM_RX bit set low, a payload in the TX FIFO and a high pulse on the CE for more than 20μs.

The RF stays in TX mode until it finishes transmitting a packet. If CE = 0, the chip returns to standby-I mode. If CE = 1, the status of the TX FIFO determines the next action. If the TX FIFO is not empty the RF remains in TX mode and transmits the next packet. If the TX FIFO is empty the chip goes into standby-II mode.

3.2.1.6 Operational modes configuration

The following (table 3.2.1.6) describes how to configure the operational modes:

Mode	PWR_UP register	PRIM_RX register	CE input pin	FIFO state
RX mode	1	1	1	-
TX mode	1	0	1	Data TX FIFO. Will empty all level in TX FIFOsa
TX mode	1	0	Minimum 20us high pulse	Data TX FIFO. Will empty one level in TX FIFOsb
Standby-2	1	0	1	TX FIFO empty
Standby-1	1	-	0	No ongoing packet transmission
Power	0	-	-	-

Down				

Table3.2.1.6 the RF main modes

a. If CE is held high all TX FIFOs are emptied and all necessary ACK and possible retransmits are carried out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when the CE is still high, the chip enters standby-II mode. In this mode the transmission of a packet is started as soon as the CSN is set high after an upload (UL) of a packet to TX FIFO.

b. This operating mode pulses the CE high for at least 20µs. This allows one packet to be transmitted. This is the normal operating mode. After the packet is transmitted, the chip enters standby-1mode.

3.2.1.7 Timing Information

The timing information in this section relates to the transitions between modes and the timing for the CE pin. The transition from TX mode to RX mode or vice versa is the same as the transition from the standby modes to TX mode or RX mode (max.210µs), as described in Table6.2

Name	The chip	Notes	Max.	Min.	Comments
Tpd2stby	Power down→Standby mode		150us		With external clock
		a	2ms		External crystal, Ls< 30Mh
			3ms		External crystal, Ls< 60Mh
			4.5ms		External crystal, Ls< 90Mh
Tstby2a	Standby mode→TX/RX mode		210us		
Thce	Minimum CE high			20us	
Tpece2csn	Delay from CE positive edge to CSN low			4us	

Table 3.2.1.7 operational timing of the RF chip

a. See crystal specifications.

For RF to go from power down mode to TX or RX mode it must first pass through stand-by mode. There must be a delay of Tpd2stby (see Table 6.2) after the RF leaves power down mode before the CE is set high.

Note: If VDD is turned off the register value is lost and you must configure chip before entering the TX or RX modes.

3.2.2 Air data rate

The air data rate is the modulated signaling rate the chip uses when transmitting and receiving data. It can be 500kbps, 1Mbps or 2Mbps. Using lower air data rate gives better receiver sensitivity than higher air data rate. But, high air data rate gives lower average current consumption and reduced probability of on-air collisions. The air data rate is set by the RF_DR bit in the RF_SETUP register. A transmitter and a receiver must be programmed with the same air data rate to communicate with each other.

3.2.3 RF channel frequency

The RF channel frequency determines the center of the channel used by the chip. The channel occupies a bandwidth of less than 1MHz at 500kbps and 1Mbps and a bandwidth of less than 2MHz at 2Mbps. The chip can operate on frequencies from 2.400GHz to2.525GHz. The programming resolution of the RF channel frequency setting is 1MHz.

At 2Mbps the channel occupies a bandwidth wider than the resolution of the RF channel frequency setting. To ensure non-overlapping channels in 2Mbps mode, the channel spacing must be 2MHz or more. At 1Mbps, the channel bandwidth is the same or lower than the resolution of the RF frequency.

The RF channel frequency is set by the RF_CH register according to the following formula:

$$F_0 = 2400 + RF\_CH\ [MHz]$$

You must program a transmitter and a receiver with the same RF channel frequency to communicate with each other.

3.2.4 Received Power Detector measurements

Received Power Detector (RPD), located in register 09, is a signed number which corresponds to different level of received power in dBm. The highest bit of RPD is sign bit. The range of the received power is -100 ~ +10dBm.

The RPD can be read out at any time while the chip is in received mode. This offers a snapshot of the current received power level in the channel. The status of RPD is correct when RX mode is enabled and after a wait time of Tstby2a +Tdelay_AGC= 210us + 20us. The RX gain varies over temperature which means that the RPD value also varies over temperature.

3.2.5 PA control

The PA (Power Amplifier) control is used to set the output power from the chip power amplifier. In TX mode PA control has four programmable steps, see Table 6.3.

The PA control is set by the PA_PWR bits in the RF_SETUP register.

SPI RF-SETUP (PA_PWR[3:0])	RF output power	DC current consumption
1000	0dBm	18.5mA
0100	-6dBm	16mA
0010	-12dBm	14mA
0001	-16dBm	12mA

Table 3.2.5 RF output power setting for the RF

Conditions: VDD = 3.0V, VSS = 0V, TA = 27ºC
Note: set PA_PWR[3:0] to 1111 can obtain maximum +6dBm output power

3.2.6 RX/TX control

The RX/TX control is set by PRIM_RX bit in the CONFIG register and sets the RF chip in transmit/receive mode.

3.3 Protocol Engine

Protocol engine is a packet based data link layer that features automatic packet assembly and timing, automatic acknowledgement and retransmissions of packets. Protocol engine enables the implementation of ultralow power and high performance communication. The Protocol engine features enable significant improvements of power efficiency for bi-directional and uni-directional systems, without adding complexity on the host controller side.

3.3.1 Features

The main features of Protocol engine are:

- 1 to 32 bytes dynamic payload length
- Automatic packet handling
- Automatic packet transaction handling
  - Auto Acknowledgement with payload
  - Auto retransmit
- 6 data pipe for 1:6 star networks

3.3.2 Protocol engine overview

Protocol engine uses self defined protocol for automatic packet handling and timing. During transmit, Protocol engine assembles the packet and clocks the bits in the data packet for transmission. During receive, Protocol engine constantly searches for a valid address in the demodulated signal. When Protocol engine finds a valid address, it processes the rest of the packet and validates it by CRC. If the packet is valid the payload is moved into a vacant slot in the RX FIFOs. All high speed bit handling and timing is controlled by protocol engine.

Protocol engine features automatic packet transaction handling for the easy implementation of a reliable bi-directional data link. A protocol engine packet transaction is a packet exchange between two transceivers, with one transceiver acting as the Primary Receiver (PRX) and the other transceiver acting as the Primary Transmitter (PTX). A protocol engine packet transaction is always initiated by a packet transmission from the PTX, the transaction is complete when the PTX has received an acknowledgment packet (ACK packet) from the PRX. The PRX can attach user data to the ACK packet enabling a bi-directional data link.

The automatic packet transaction handling works as follows:

1. You begin the transaction by transmitting a data packet from the PTX to the PRX. Protocol engine automatically sets the PTX in receive mode to wait for the ACK packet.
2. If the packet is received by the PRX, Protocol engine automatically assembles and transmits an acknowledgment packet (ACK packet) to the PTX before returning to receive mode.

3. If the PTX does not receive the ACK packet immediately, Protocol engine automatically retransmits the original data packet after a programmable delay and sets the PTX in receive mode to wait for the ACK packet.

In Protocol engine it is possible to configure parameters such as the maximum number of retransmits and the delay from one transmission to the next retransmission. All automatic handling is done without the involvement of the MCU.

3.3.3 Protocol engine packet format

The format of the Protocol engine packet is described in this section. The Protocol engine packet contains a preamble field, address field, packet control field, payload field and a CRC field. Figure3.3.3 shows the packet format with MSB to the left.

Preamble 1 byte	Address 4-5 byte	2byte guard	Packet control field 9 bit	Payload 0-32 bytes	CRC 1-2 bytes

Figure3.3.3 A Protocol engine packet with payload (0-32 bytes)

3.3.3.1 Preamble

The preamble is a bit sequence used to synchronize the receivers demodulator to the incoming bit stream. The preamble is one byte long and is either 01010101 or 10101010. If the first bit in the address is 1 the preamble is automatically set to 10101010 and if the first bit is 0 the preamble is automatically set to 01010101. This is done to ensure there are enough transitions in the preamble to stabilize the receiver.

3.3.3.2 Address

This is the address for the receiver. An address ensures that the packet is detected and received by the correct receiver, preventing accidental cross talk between multiple RF systems. You can configure the address field width in the AW register to be 5 bytes or 4 bytes address.

3.3.3.3 Guard

Figure 3.3.3 shows the format of the 2 bytes guard packet has better synchronous characteristics.

3.3.3.4 Packet Control Field (PCF)

Figure 3.4.4 shows the format of the 9 bit packet control field, MSB to the left.

Payload length 6bit	PID 2bit	NO_ACK 1bit

Figure 3.4.4 Packet control field (PCF)

The packet control field contains a 6 bit payload length field, a 2 bit PID (Packet Identity) field and a 1 bit NO_ACK flag.

3.3.3.4.1 Payload length

This 6 bit field specifies the length of the payload in bytes. The length of the payload can be from 0 to 32 bytes.

Coding: 000000 = 0 byte (only used in empty ACK packets. The 0 length packet also need to be read out use R_RX_PAYLOAD with no data following) 100000 = 32 byte, 100001 = Don't care.

This field is only used if the Dynamic Payload Length function is enabled.

3.3.3.4.2 PID (Packet identification)

The 2 bit PID field is used to detect if the received packet is new or retransmitted. PID prevents the PRX operation from presenting the same payload more than once to the MCU. The PID field is incremented at the TX side for each new packet received through the SPI. The PID and CRC field are used by the PRX operation to determine if a packet is retransmitted or new. When several data packets are lost on the link, the PID fields may become equal to the last received PID. If a packet has the same PID as the previous packet, the RF transceiver compares the CRC sums from both packets. If the CRC sums are also equal, the last received packet is considered a copy of the previously received packet and discarded.

3.3.3.4.3 No Acknowledgment flag (NO_ACK)

The Selective Auto Acknowledgement feature controls the NO_ACK flag.

This flag is only used when the auto acknowledgement feature is used. Setting the flag high, tells the receiver that the packet is not to be auto acknowledged.

On the PTX you can set the NO_ACK flag bit in the Packet Control Field with this command:
W_TX_PAYLOAD_NOACK

However, the function must first be enabled in the FEATURE register by setting the EN_DYN_ACK bit. When you use this option, the PTX goes directly to standby-I mode after transmitting the packet. The PRX does not transmit an ACK packet when it receives the packet.

3.3.3.5 Payload

The payload is the user defined content of the packet. It can be 0 to 32 bytes wide and is transmitted on-air when it is uploaded to the device.

Protocol engine provides two alternatives for handling payload lengths; static and dynamic.

The default is static payload length. With static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by the RX_PW_Px registers on the receiver side. The payload length on the transmitter side is set by the number of bytes clocked into the TX_FIFO and must equal the value in the RX_PW_Px register on the receiver side.

Dynamic Payload Length (DPL) is an alternative to static payload length. DPL enables the transmitter to send packets with variable payload length to the receiver. This means that for a system with different payload lengths it is not necessary to scale the packet length to the longest payload.

With the DPL feature the RF can decode the payload length of the received packet automatically instead of using the RX_PW_Px registers. The MCU can read the length of the received payload by using the R_RX_PL_WID command.

Note: Always check if the packet width reported is 32 bytes or shorter when using the R_RX_PL_WID command. If its width is longer than 32 bytes then the packet contains errors and must be discarded. Discard the packet by using the Flush_RX command.

In order to enable DPL the EN_DPL bit in the FEATURE register must be enabled. In RX mode the DYNPD register must be set. A PTX that transmits to a PRX with DPL enabled must have the DPL_P0 bit in DYNPD set.

3.3.3.6 CRC (Cyclic Redundancy Check)

The CRC is the error detection mechanism in the packet. It may either be 1 or 2 bytes and is calculated over the address, Packet Control Field and Payload.

The polynomial for 1 byte CRC is X8 + X2 + X + 1. Initial value 0Xff.

The polynomial for 2 byte CRC is X16 + X12 + X5 + 1. Initial value 0Xffff.

The number of bytes in the CRC is set by the CRCO bit in the CONFIG register. No packet is accepted by protocol engine if the CRC fails.

3.3.3.7 Automatic packet assembly

The automatic packet assembly assembles the preamble, address, packet control field, payload and CRC to make a complete packet before it is transmitted.

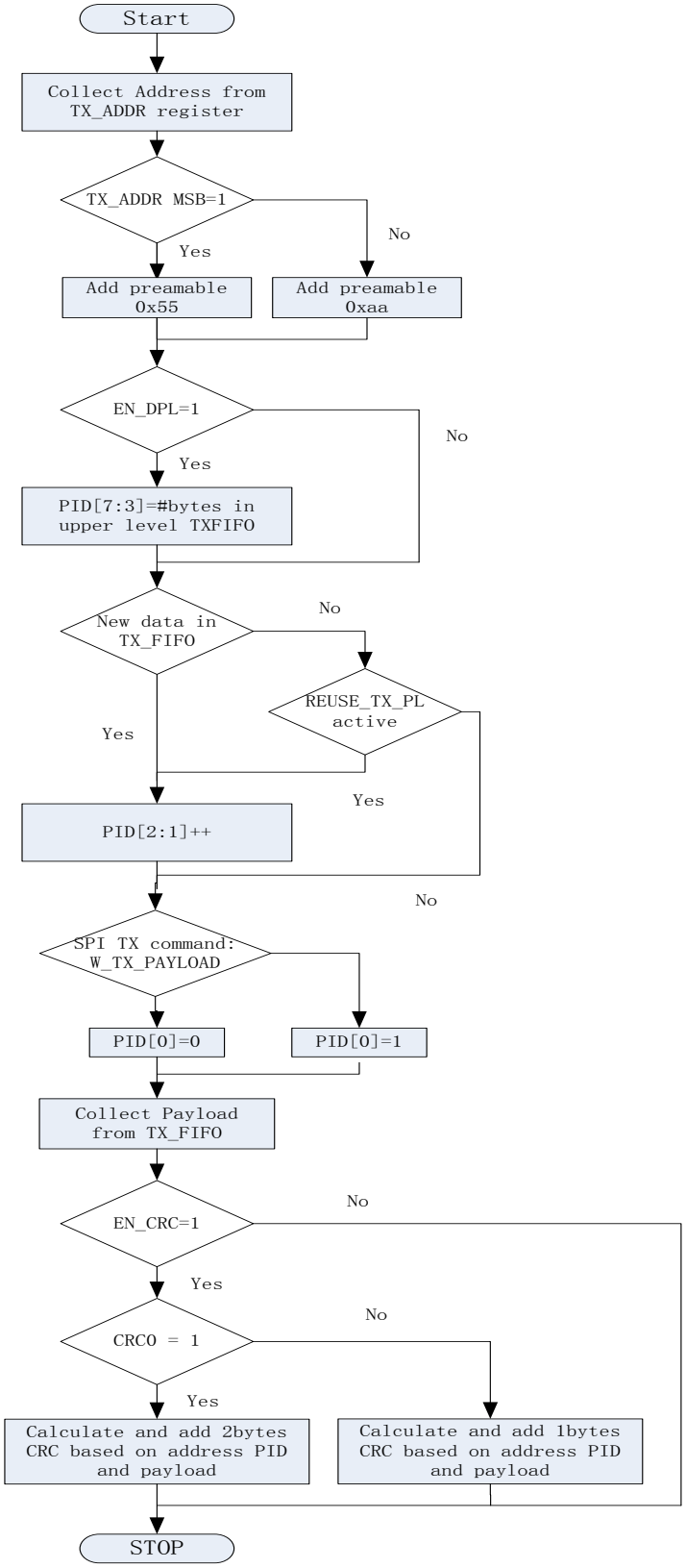


Figure 3.3.3.7 Automatic packet assembly

3.3.3.8 Automatic packet disassembly

After the packet is validated, Protocol engine disassembles the packet and loads the payload into the RX FIFO, and asserts the RX_DR IRQ.

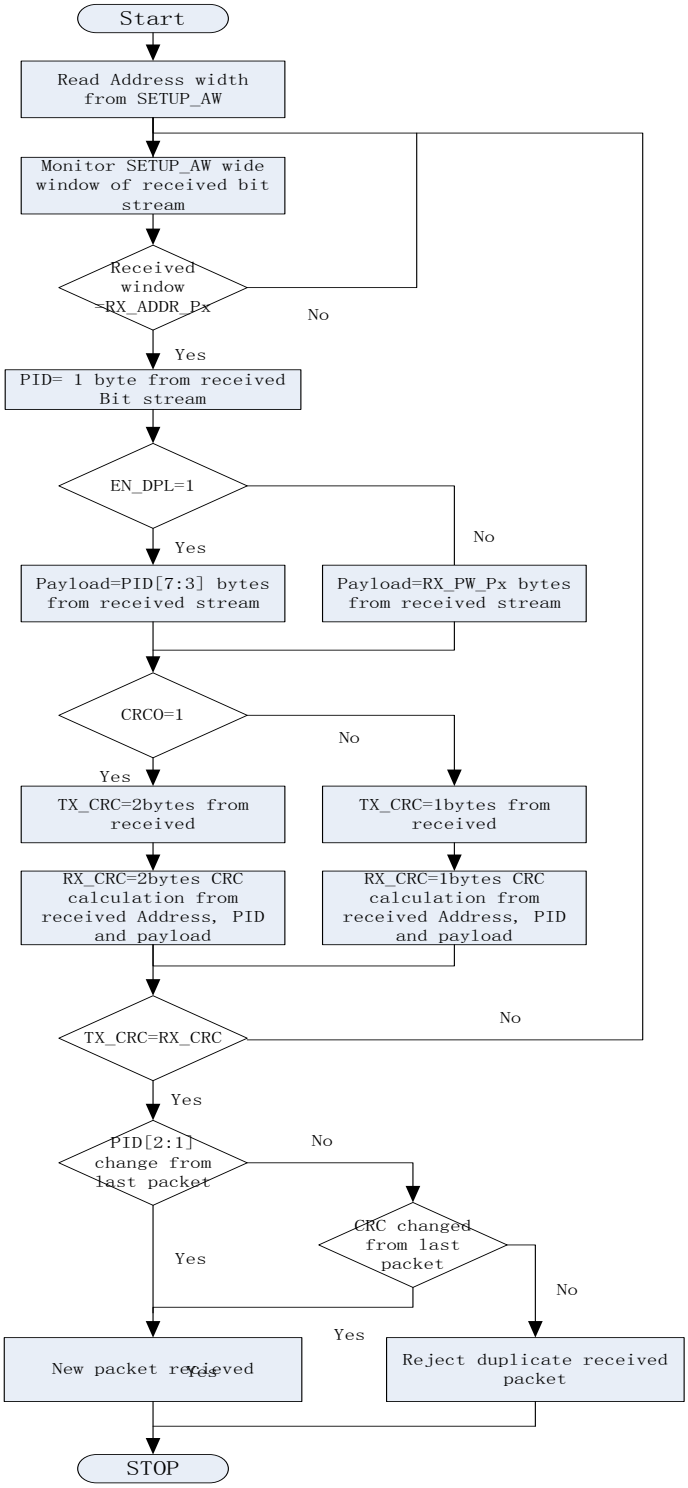


Figure 3.3.3.8 Automatic packet disassembly

3.3.4 Automatic packet transaction handling

Protocol engine features two functions for automatic packet transaction handling; auto acknowledgement and auto re-transmit.

3.3.4.1 Auto Acknowledgement

Auto Acknowledgment is a function that automatically transmits an ACK packet to the PTX after it has received and validated a packet. The Auto Acknowledgement function reduces the load of the system MCU and reduces average current consumption. The Auto Acknowledgement feature is enabled by setting the EN_AA register.

Note: If the received packet has the NO_ACK flag set, auto acknowledgement is not executed.

An ACK packet can contain an optional payload from PRX to PTX. In order to use this feature, the Dynamic Payload Length (DPL) feature must be enabled. The MCU on the PRX side has to upload the payload by clocking it into the TX FIFO by using the W_ACK_PAYLOAD command. The payload is pending in the TX FIFO (PRX) until a new packet is received from the PTX. The RF transceiver can have three ACK packet payloads pending in the TX FIFO (PRX) at the same time.

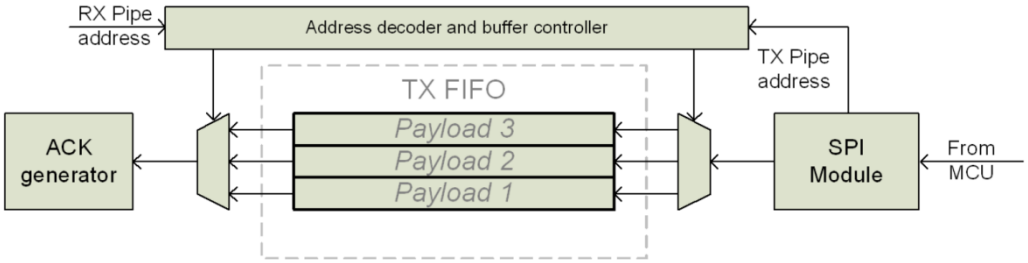


Figure 3.3.4.1 TX FIFO (PRX) with pending payloads

Figure 3.3.4.1shows how the TX FIFO (PRX) is operated when handling pending ACK packet payloads. From the MCU the payload is clocked in with the W_ACK_PAYLOAD command. The address decoder and buffer controller ensure that the payload is stored in a vacant slot in the TX FIFO (PRX). When a packet is received, the address decoder and buffer controller are notified with the PTX address. This ensures that the right payload is presented to the ACK generator.

If the TX FIFO (PRX) contains more than one payload to a PTX, payloads are handled using the first in–first out principle. The TX FIFO (PRX) is blocked if all pending payloads are addressed to a PTX where the link is lost. In this case, the MCU can flush the TX FIFO (PRX) by using the FLUSH_TX command.

In order to enable Auto Acknowledgement with payload the EN_ACK_PAY bit in the FEATURE register must be set.

3.3.4.2 Auto Retransmission (ART)

The auto retransmission is a function that retransmits a packet if an ACK packet is not received. It is used in an Auto Acknowledgement system on the PTX. When a packet is not acknowledged, you can set the number of times it is allowed to retransmit by setting the ARC bits in the SETUP_RETR register. PTX enters RX mode and waits a time period for an ACK packet each time a packet is transmitted. The amount of time the PTX is in RX mode is based on the following conditions:

- Auto Retransmit Delay (ARD) has elapsed.
- No address match within 256 µs.
- After received packet (CRC correct or not) if address match within 256 µs.

The RF transceiver asserts the TX_DS IRQ when the ACK packet is received.

The RF transceiver enters standby-I mode if there is no more un-transmitted data in the TX FIFO and the CE pin is low. If the ACK packet is not received, the RF transceiver goes back to TX mode after a delay defined by ARD and retransmits the data. This continues until acknowledgment is received, or the maximum number of retransmits is reached.

Two packet loss counters are incremented each time a packet is lost, ARC_CNT and PLOS_CNT in the OBSERVE_TX register. The ARC_CNT counts the number of retransmissions for the current transaction. You reset ARC_CNT by initiating a new transaction. The PLOS_CNT counts the total number of retransmissions since the last channel change. You reset PLOS_CNT by writing to the RF_CH register. It is possible to use the information in the OBSERVE_TX register to make an overall assessment of the channel quality.

The ARD defines the time from the end of a transmitted packet to when a retransmit starts on the PTX. ARD is set in SETUP_RETR register in steps of 256µs. A retransmit is made if no ACK packet is received by the PTX.

There is a restriction on the length of ARD when using ACK packets with payload. The ARD time must never be shorter than the sum of the startup time and the time on-air for the ACK packet.

- For 2 Mbps data rate and 5-byte address; 15 byte is maximum ACK packet payload length for ARD=256µs (reset value).
- For 1 Mbps data rate and 5-byte address; 5 byte is maximum ACK packet payload length for ARD=256µs (reset value).

ARD=512µs is long enough for any ACK payload length in 1 or 2 Mbps mode.

- For 500kbps data rate and 5-byte address the following values apply:

ARD	ACK packet size (in byte)
1536us	All ACK payload sizes
1280us	<=24
1024us	<=16
768us	<=8
512us	Empty ACK with no payload

Table 3.3.4.2 Maximum ACK payload length for different retransmit delays

As an alternative to Auto Retransmit it is possible to manually set the RF transceiver to retransmit a packet a number of times. This is done by the REUSE_TX_PL command. The MCU must initiate each transmission of the packet with a pulse on the CE pin when this command is used.

3.3.5 Protocol engine flowcharts

This section contains flowcharts outlining PTX and PRX operation in Protocol engine.

3.3.5.1 PTX operation

The flowchart in Figure 3.3.5.1 outlines how a RF transceiver configured as a PTX behaves after entering standby-I mode.

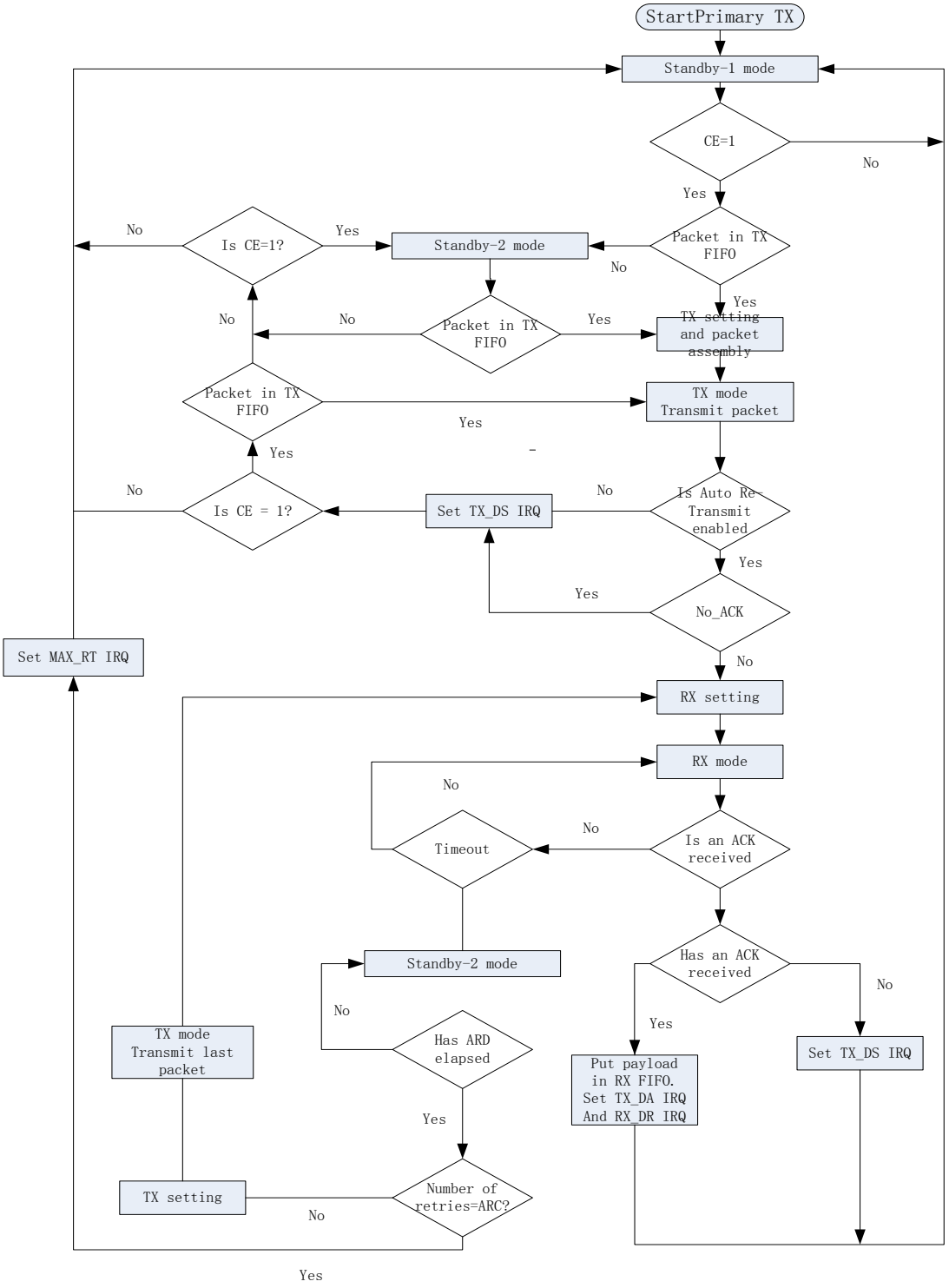


Figure 3.3.5.1 PTX operations in Protocol engine

Note: Protocol engine operation is outlined with a dashed square.

Activate PTX mode by setting the CE high. If there is a packet present in the TX FIFO the RF transceiver enters TX mode and transmits the packet. If Auto Retransmit is enabled, the state machine checks if the NO_ACK flag is set. If it is not set, the RF transceiver enters RX mode to receive an ACK packet. If the received ACK packet is empty, only the TX_DS IRQ is asserted. If the ACK packet contains a payload, both TX_DS IRQ and RX_DR IRQ are asserted simultaneously before the RF transceiver returns to standby-I mode.

If the ACK packet is not received before timeout occurs, the RF transceiver returns to standby-II mode. It stays in standby-II mode until the ARD has elapsed. If the number of retransmits has not reached the ARC, the RF transceiver enters TX mode and transmits the last packet once more.

While executing the Auto Retransmit feature, the number of retransmits can reach the maximum number defined in ARC. If this happens, the RF transceiver asserts the MAX_RT IRQ and returns to standby-I mode.

If the CE bit in the RFCON register is high and the TX FIFO is empty, the RF transceiver enters Standby-II mode.

3.3.5.2 PRX operation

The flowchart in Figure 3.3.5.2 outlines how a RF transceiver configured as a PRX behaves after entering standby-I mode.

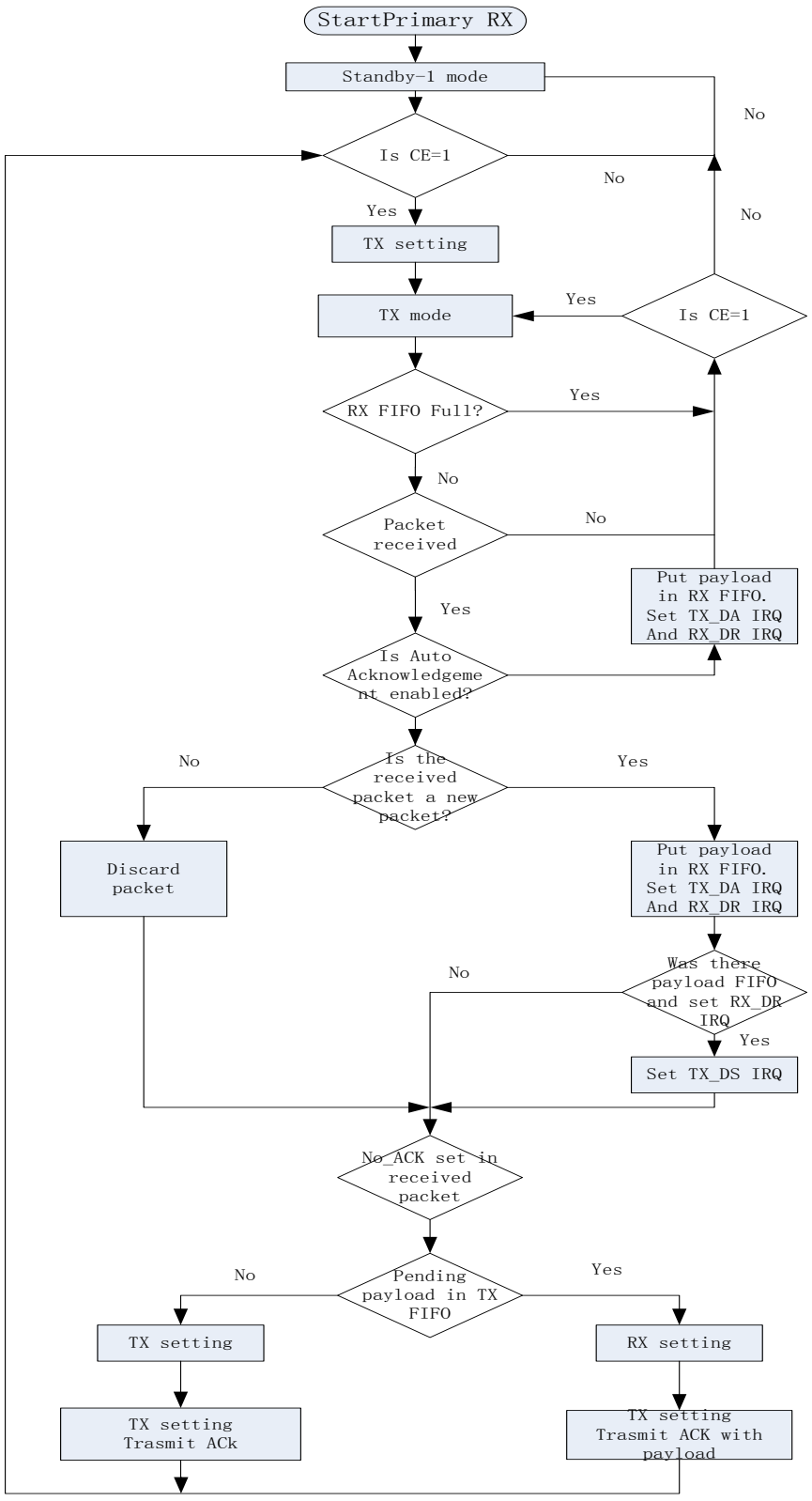


Figure3.3.5.2 PRX operations in Protocol engine

Note: Protocol engine operation is outlined with a dashed square.

Activate PRX mode by setting the CE bit in the RFCON register high. The RF transceiver enters RX mode and starts searching for packets. If a packet is received and Auto Acknowledgement is enabled, the RF transceiver decides if the packet is new or a copy of a previously received packet. If the packet is new payload is made available in the RX FIFO and the RX_DR IRQ is asserted. If the last received packet from the transmitter is acknowledged with an ACK packet with payload, the TX_DS IRQ indicates that the PTX received the ACK packet with payload. If the No_ACK flag is not set in the received packet, the PRX enters

TX mode. If there is a pending payload in the TX FIFO it is attached to the ACK packet. After the ACK packet is transmitted, the RF transceiver returns to RX mode.

A copy of a previously received packet might be received if the ACK packet is lost. In this case, the PRX discards the received packet and transmits an ACK packet before it returns to RX mode.

3.3.6 MultiSlave

MultiSlave is a feature used in RX mode that contains a set of six parallel data pipes with unique addresses. A data pipe is a logical channel in the physical RF channel. Each data pipe has its own physical address (data pipe address) decoding in the RF transceiver.

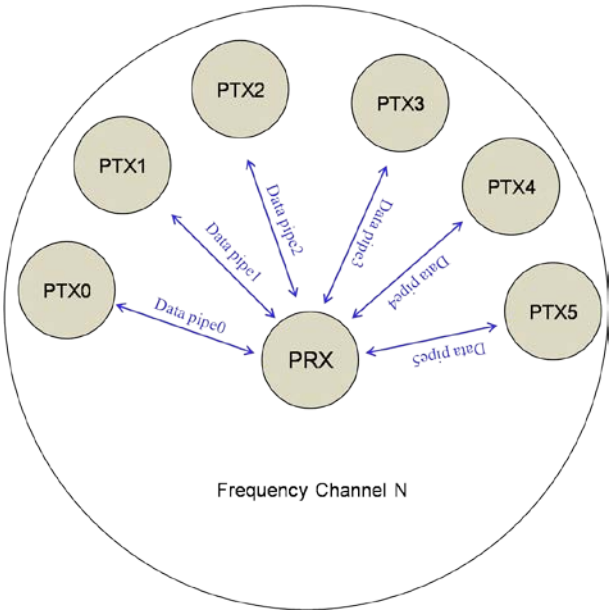


Figure3.3.6.1 PRX using MultiSlave

The RF transceiver configured as PRX (primary receiver) can receive data addressed to six different data pipes in one frequency channel. Each data pipe has its own unique address and can be configured for individual behavior.

Up to six RF transceivers configured as PTX can communicate with one RF transceiver configured as PRX. All data pipe addresses are searched for simultaneously. Only one data pipe can receive a packet at a time. All data pipes can perform Protocol engine functionality.

The following settings are common to all data pipes:

- CRC enabled/disabled (CRC always enabled when Protocol engine is enabled)
- CRC encoding scheme
- RX address width
- Frequency channel
- Air data rate
- LNA gain

The data pipes are enabled with the bits in the EN_RXADDR register. By default only data pipe 0 and 1 are enabled. Each data pipe address is configured in the RX_ADDR_PX registers.

Note: Always ensure that none of the data pipes have the same address.

Each pipe can have up to a 5 byte configurable address. Data pipes 0-5 share the four most significant address bytes. The LSByte must be unique for all six pipes. Figure 3.3.6.2 is an example of how data pipes 0-5 are addressed. Only pipe0 can have up to a 5 byte configurable address, other's pipes have 1bytes configurable address.

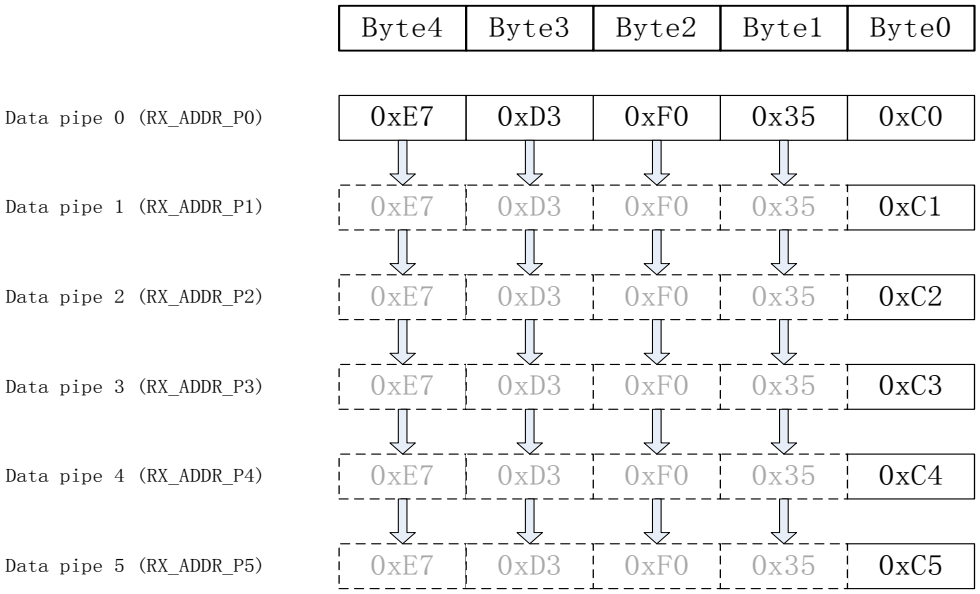


Figure 3.3.6.2 Addressing data pipes 0-5

The PRX, using MultiSlave and Protocol engine, receives packets from more than one PTX. To ensure that the ACK packet from the PRX is transmitted to the correct PTX, the PRX takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet. Figure 3.3.6.3 is an example of an address configuration for the PRX and PTX. On the PRX the RX_ADDR_Px, defined as the pipe address, must be unique. On the PTX the TX_ADDR must be the same as the RX_ADDR_P0 and as the pipe address for the designated pipe.

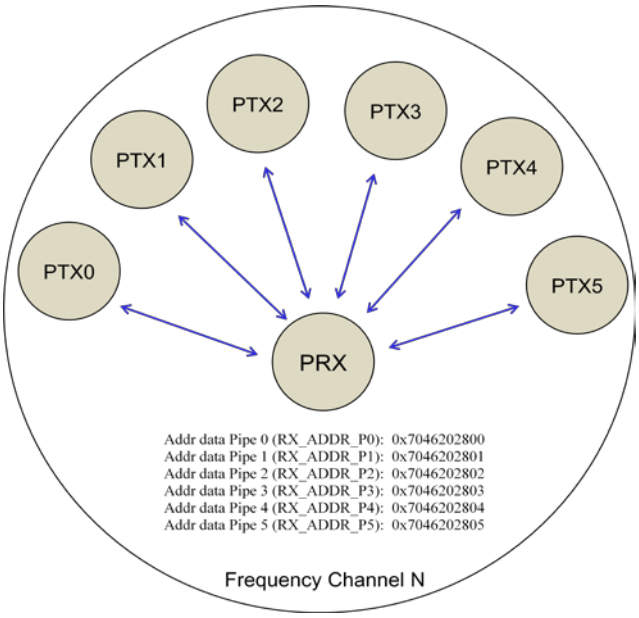
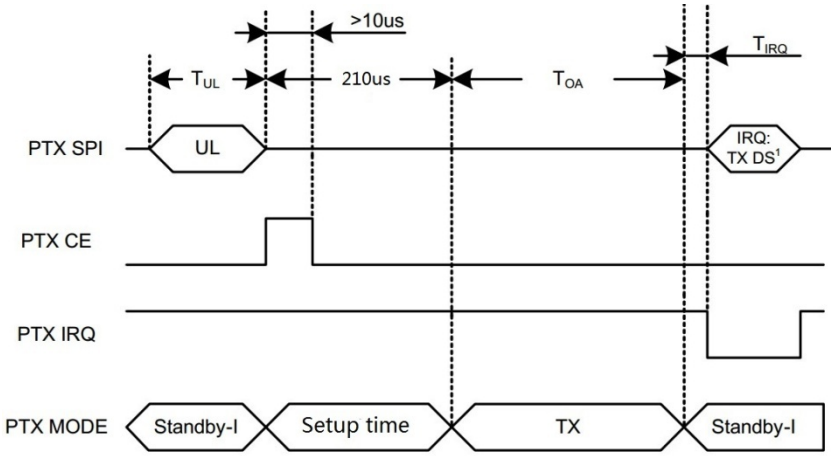


Figure 3.3.6.3Example of data pipe addressing in MultiSlave

Only when a data pipe receives a complete packet can other data pipes begin to receive data. When multiple PTXs are transmitting to a PRX, the ARD can be used to skew the auto retransmission so that they only block each other once.

3.3.7 Protocol engine timing

This section describes the timing sequence of Protocol engine and how all modes are initiated and operated. The Protocol engine timing is controlled through the Data and Control interface. The RF transceiver can be set to static modes or autonomous modes where the internal state machine controls the events. Each autonomous mode/sequence ends with a RFIRQ interrupt. All the interrupts are indicated as IRQ events in the timing diagrams.



1 IRQ if No Ack is on.

TIRQ=3us @ 1Mbps, @2Mbps

Figure 3.3.7.1Transmitting one packet with NO_ACK on

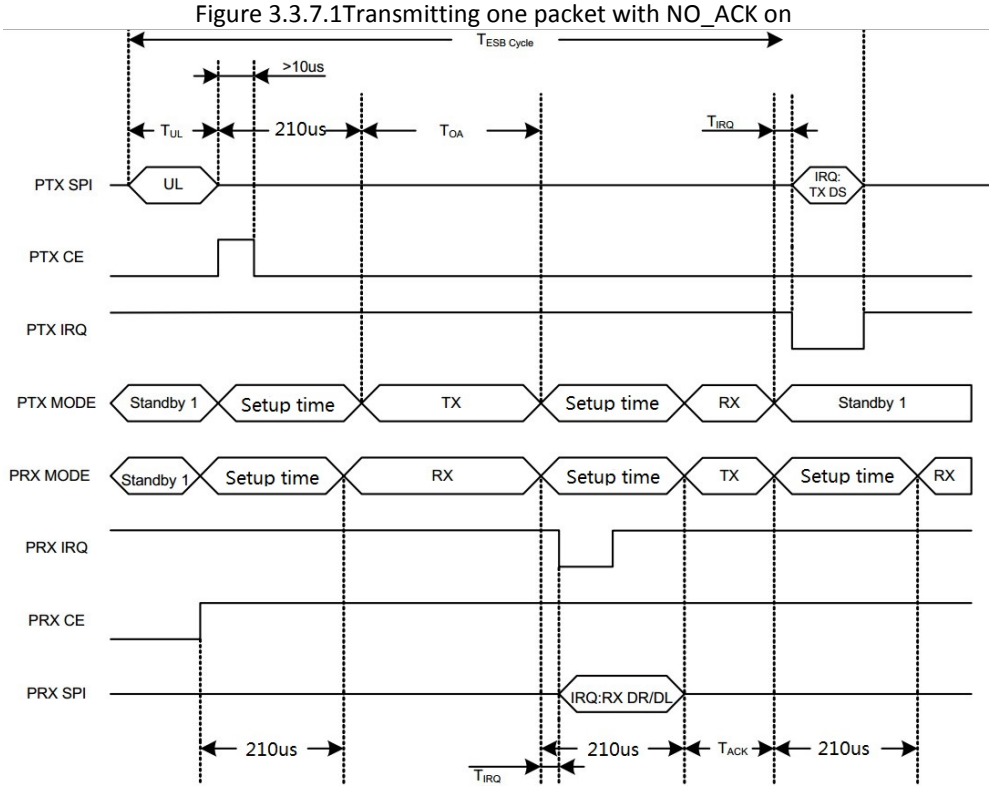


Figure 3.3.7.2 Timing of Protocol engine for one packet upload (2Mbps)

In Figure 3.3.7.2, the transmission and acknowledgement of a packet is shown. The PRX operation activates RX mode (CE=1), and the PTX operation is activated in TX mode (CE=1 for minimum 20μs). After 210μs the transmission starts and finishes after the elapse of TOA.

When the transmission ends the PTX operation automatically switches to RX mode to wait for the ACK packet from the PRX operation. When the PRX operation receives the packet it sets the interrupt for the

host MCU and switches to TX mode to send an ACK. After the PTX operation receives the ACK packet it sets the interrupt to the MCU and clears the packet from the TX FIFO.

In Figure 3.3.7.3, the PTX timing of a packet transmission is shown when the first ACK packet is lost.

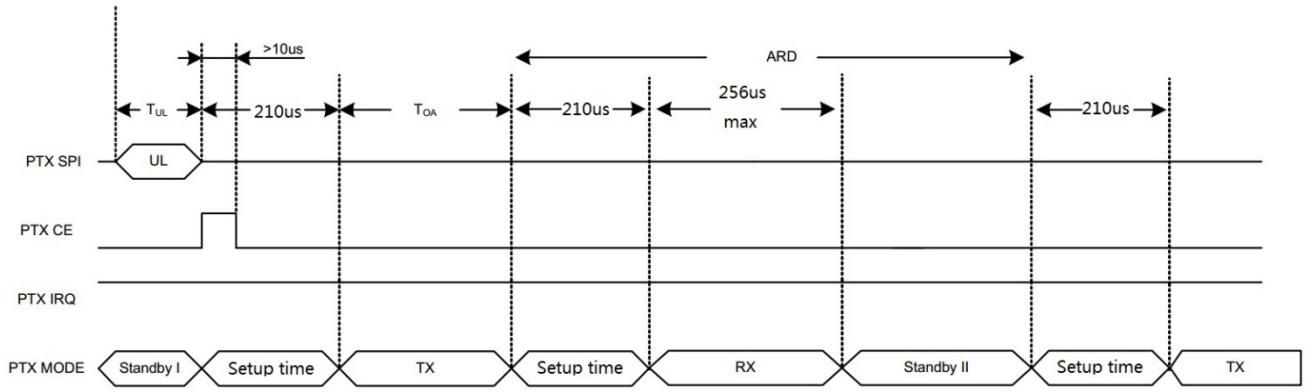


Figure 3.3.7.3Timing of Protocol engine when the first ACK packet is lost (2 Mbps)

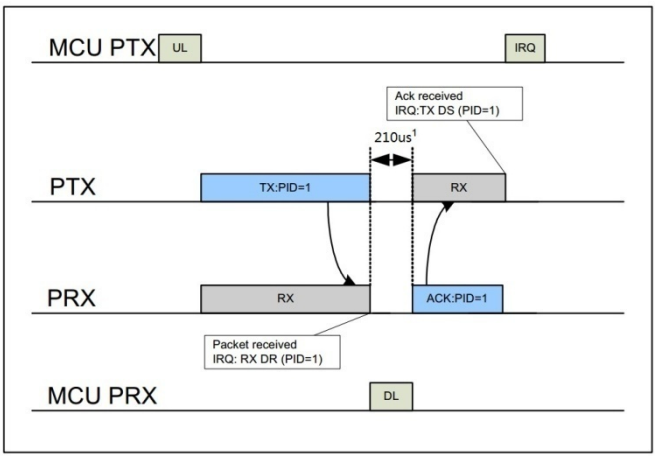
3.3.8 Protocol engine transaction diagram

This section describes several scenarios for the Protocol engine automatic transaction handling. The call outs in this section's figures indicate the IRQs and other events. For MCU activity the event may be placed at a different timeframe.

Note: The figures in this section indicate the earliest possible download (DL) of the packet to the MCU and the latest possible upload (UL) of payload to the transmitter.

3.3.8.1 Single transaction with ACK packet and interrupts

In Figure 3.3.8.1, the basic auto acknowledgement is shown. After the packet is transmitted by the PTX and received by the PRX the ACK packet is transmitted from the PRX to the PTX. The RX_DR IRQ is asserted after the packet is received by the PRX, whereas the TX_DS IRQ is asserted when the packet is acknowledged and the ACK packet is received by the PTX.



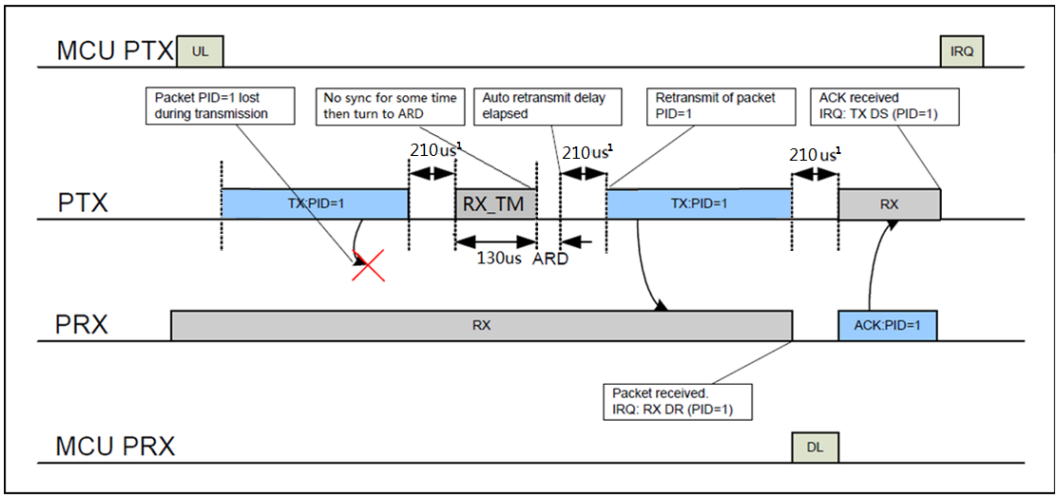
1 Radio Turn Around delay

Figure 3.3.8.1 TX/RX cycles with ACK and the according interrupts

3.3.8.2 Single transaction with a lost packet

Figure 3.3.8.2 is a scenario where a retransmission is needed due to loss of the first packet transmits. After the packet is transmitted, the PTX enters RX mode to receive the ACK packet. After the first transmission, the PTX waits a specified time (including setup time, RX_TM and ARD) for the ACK packet, if it is not in the specific time slot the PTX retransmits the packet as shown in Figure 7.15. PTX will turn to RX

mode after 210us setup time when packet is transmitted, after 130us RX timeout (RX_TM is RX timeout for PTX, it can be set shorter), then PTX turn to ARD (can be set to 0us, 256us, 512us to 3840us).



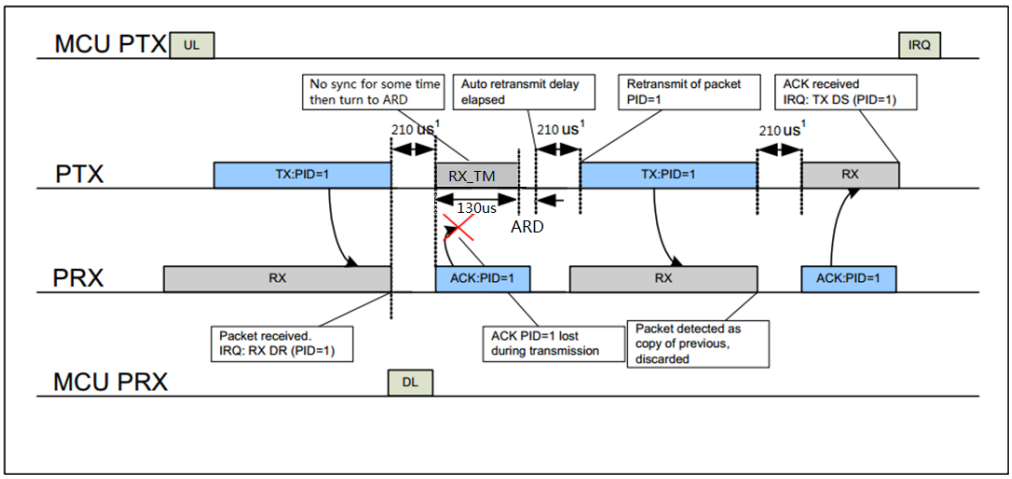
1 Radio Turn Around delay

Figure 3.3.8.2TX/RX cycles with ACK and the according interrupts when the first packet transmit fails

When an address is detected the PTX stays in RX mode until the packet is received. When the retransmitted packet is received by the PRX. The RX_DR IRQ is asserted and an ACK is transmitted back to the PTX. When the ACK is received by the PTX, the TX_DS IRQ is asserted.

3.3.8.3 Single transaction with a lost ACK packet

Figure 3.3.8.3 is a scenario where a retransmission is needed after a loss of the ACK packet. The corresponding interrupts are also indicated.

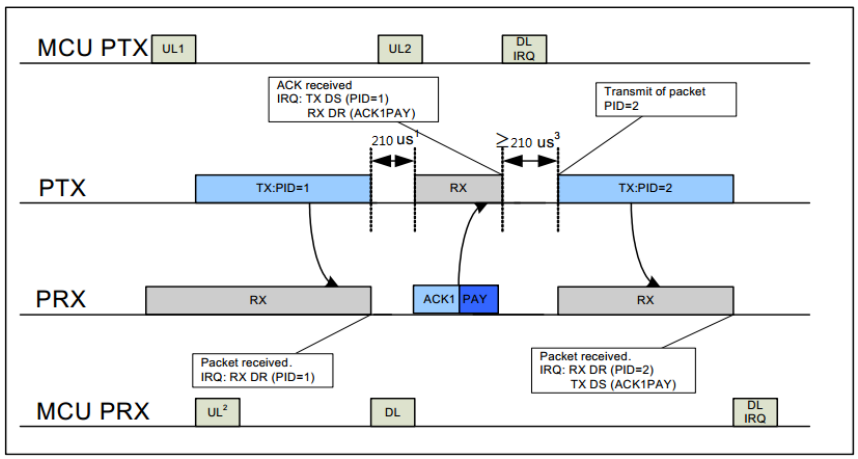


1 Radio Turn Around delay

Figure 3.3.8.3TX/RX cycles with ACK and the according interrupts when the ACK packet fails

3.3.8.4 Single transaction with ACK payload packet

Figure 3.3.8.4 is a scenario of the basic auto acknowledgement with payload. After the packet is transmitted by the PTX and received by the PRX the ACK packet with payload is transmitted from the PRX to the PTX. The RX_DR IRQ is asserted after the packet is received by the PRX, whereas on the PTX side the TX_DS IRQ is asserted when the ACK packet is received by the PTX. On the PRX side, the TX_DS IRQ for the ACK packet payload is asserted after a new packet from PTX is received. The position of the IRQ in Figure 3.3.8.4 shows where the MCU can respond to the interrupt.

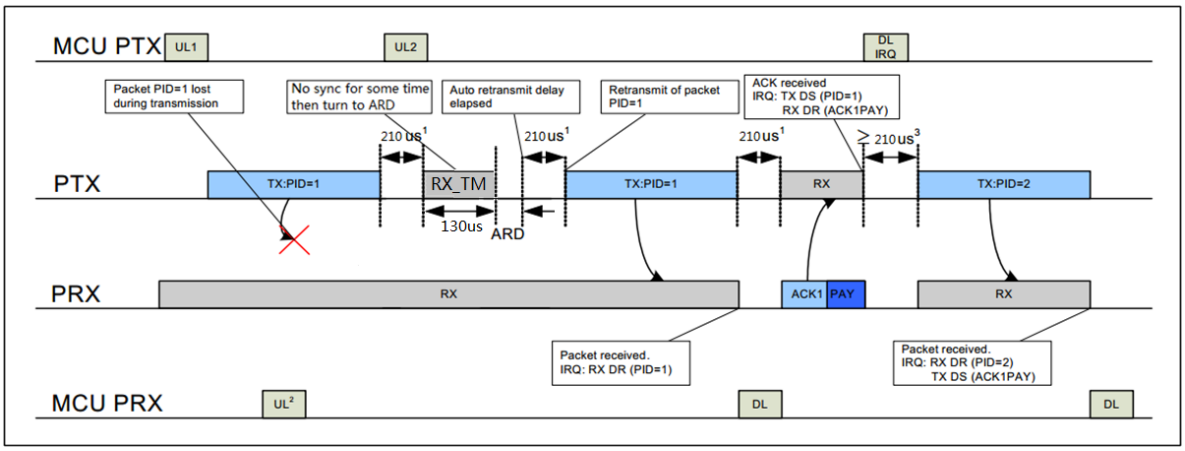


1 Radio Turn Around delay
2 Uploading payload for Ack Packet
3 Delay defined by MCU on PTX side, >=210us

Figure 3.3.8.4 TX/RX cycles with ACK Payload and the according interrupts

3.3.8.5 Single transaction with ACK payload packet and lost packet

Figure 3.3.8.5 is a scenario where the first packet is lost and a retransmission is needed before the RX_DR IRQ on the PRX side is asserted. For the PTX both the TX_DS and RX_DR IRQ are asserted after the ACK packet is received. After the second packet (PID=2) is received on the PRX side both the RX_DR (PID=2) and TX_DS (ACK packet payload) IRQ are asserted.

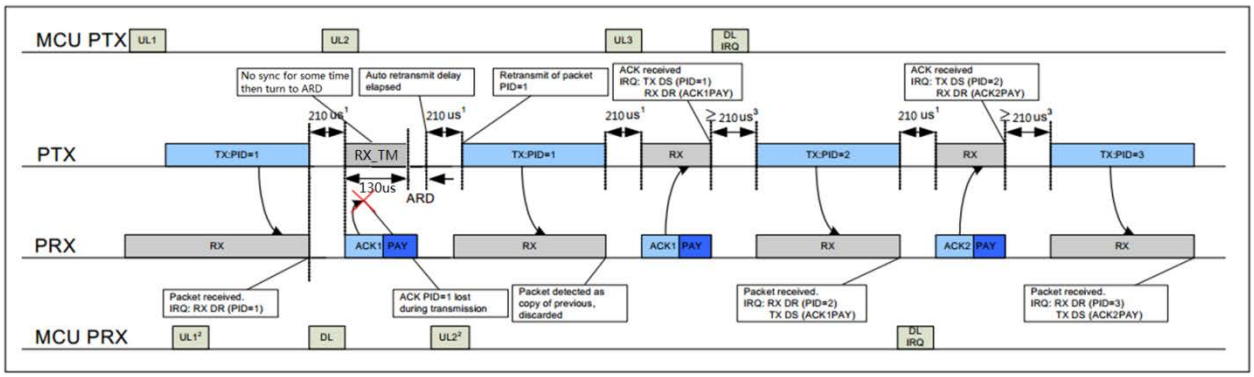


1 Radio Turn Around delay
2 Uploading payload for Ack Packet
3 Delay defined by MCU on PTX side, >=210us

Figure 3.3.8.5 TX/RX cycles and the according interrupts when the packet transmission fails

3.3.8.6 Two transactions with ACK payload packet and the first ACK packet lost

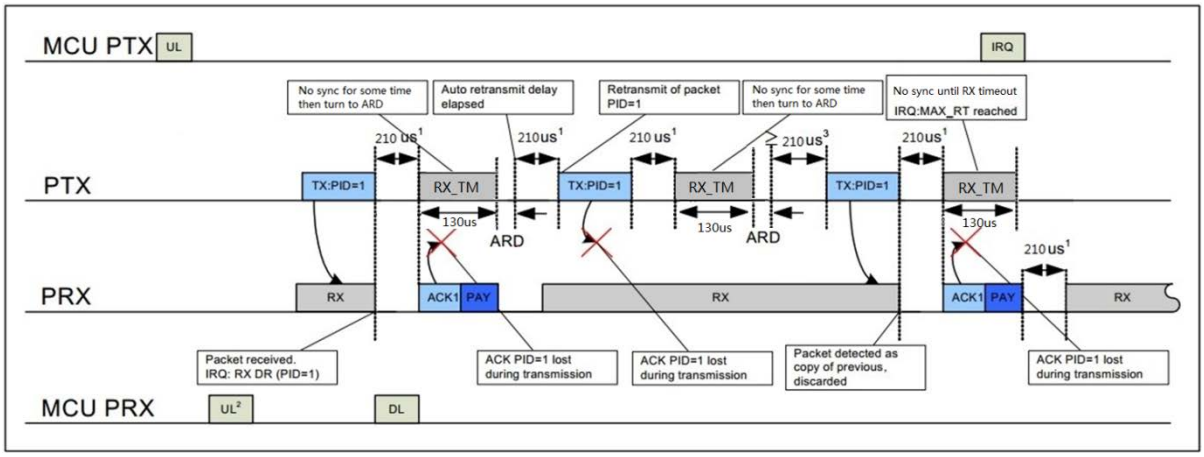
Figure 3.3.8.6 the ACK packet is lost and a retransmission is needed before the TX_DS IRQ is asserted, but the RX_DR IRQ is asserted immediately. The retransmission of the packet (PID=1) results in a discarded packet. For the PTX both the TX_DS and RX_DR IRQ are asserted after the second transmission of ACK, which is received. After the second packet (PID=2) is received on the PRX both the RX_DR (PID=2) and TX_DS (ACK1PAY) IRQ is asserted. The callouts explains the different events and interrupts.



1 Radio Turn Around delay
2 Uploading payload for Ack Packet
3 Delay defined by MCU on PTX side, >=210us

Figure 3.3.8.6 TX/RX cycles with ACK Payload and the according interrupts when the ACK packet fails

3.3.8.7 Two transactions where max retransmissions is reached



1 Radio Turn Around delay
2 Uploading payload for Ack Packet
3 Delay defined by MCU on PTX side, >=210us

Figure 3.3.8.7 TX/RX cycles with ACK Payload and the according interrupts when the transmission fails. ARC is set to 2.

MAX_RT IRQ is asserted if the auto-retransmit counter (ARC_CNT) exceeds the programmed maximum limit (ARC). In Figure 3.3.8.7, the packet transmission ends with a MAX_RT IRQ. The payload in TX FIFO is NOT removed and the MCU decides the next step in the protocol. A toggle of the CE bit in the RFCON register starts a new transmitting sequence of the same packet. The payload can be removed from the TX FIFO using the FLUSH_TX command.

3.4 Data and control interface

The data and control interface gives you access to all the features in the RF transceiver. The data and control interface consists of the following six 5Volt tolerant digital signals:

- IRQ (this signal is active low and controlled by three mask-able interrupt sources)
- CE (this signal is active high and used to activate the chip in RX or TX mode)
- CSN (SPI signal)
- SCK (SPI signal)
- MOSI (SPI signal)

- MISO (SPI signal)

Using 1 byte SPI commands, you can activate the RF data FIFOs or the register map during all modes of operation.

3.4.1 Features

- Special SPI commands for quick access to the most frequently used features
- 0-10Mbps 4-wire SPI
- 8 bit command set
- Easily configurable register map
- Full three level FIFO for both TX and RX direction

3.4.2 Functional description

The SPI is a standard SPI with a maximum data rate of 10Mbps.

3.4.3 SPI operation

This section describes the SPI commands and timing.

3.4.3.1 SPI commands

The SPI commands are shown in Table 8.1. Every new command must be started by a high to low transition on CSN.

The STATUS register is serially shifted out on the MISO pin simultaneously to the SPI command word shifting to the MOSI pin.

The serial shifting SPI commands is in the following format:

<**Command word**: MSBit to LSBit (one byte)>

<**Data bytes:** LSByte to MSByte, MSBit in each byte first>

See Figure 3.4.3.2.1 and Figure 3.4.3.2.2 for timing information.

Command	Command word (binary)	#Data bytes	Operation
R_REGISTER	000A AAAA	1 to 5 LSByte first	Read command and status registers. AAAAA=5 bit register map address
W_REGISTER	001A AAAA	1 to 5 LSByte first	Write command and status registers. AAAAA=5 bit register map address Executable in power down or standby modes only.
R_TX_PAYLOAD	0110 0001	1 to 32 LSByte first	Read RX-payload: 1-32 bytes. A read operation always starts at byte 0. Payload is deleted from FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32 LSByte first	Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0 used in TX payload.
FLUSH	1110	0	Flush TX FIFO, used in TX mode

_TX	0001		
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode Should not be executed during transmission of acknowledge, that is, acknowledge package will not be completed
REUSE_TX_PL	1110 0011	0	Used for a PTX operation Reuse last transmitted payload. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX payload reuse must not be activated or deactivated during package transmission.
R_RX_PL_WID	0110 0000	1	Read RX payload width for the top R_RX_PAYLOAD in the RX FIFO. Note: Flush RX FIFO if the read value is larger than 32 bytes.
W_ACK_PAYLOAD	1010 1PPP	1 to 32 LSByte first	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled using first in – first out principle. Write payload: 1– 32 bytes. A write operation always starts at byte 0.
W_TX_PAYLOAD_NO_ACK	1011 0000	1 to 32 LSByte first	Used in TX mode. Disables AUTOACK on this specific packet specific packet.
NOP	1111 1111	0	No Operation. Might be used to read the STATUS register

Table 3.4.3.1 Command set for the RF transceiver SPI

The W_REGISTER and R_REGISTER commands operate on single or multi-byte registers. When accessing multi-byte registers read or write to the MSBit of LSByte first. You can terminate the writing before all bytes in a multi-byte register are written, leaving the unwritten MSByte(s) unchanged. For example, the LSByte of RX_ADDR_P0 can be modified by writing only one byte to the RX_ADDR_P0 register. The content of the status register is always read to MISO after a high to low transition on CSN.

Note: The 3 bit pipe information in the STATUS register is updated during the IRQ high to low transition. The pipe information is unreliable if the STATUS register is read during an IRQ high to low transition.

3.4.3.2 SPI timing

SPI operation and timing is shown in this section. RFmust be in a standby or power down mode before writing to the configuration registers.

In Figure 3.4.3.2.1 to Figure 3.4.3.2.2 the following abbreviations are used:

Abbreviation	Description
Cn	SPI command bit
Sn	STATUS register bit
Dn	Data Bit (Note: LSByte to MSByte, MSBit in each byte first)

Table 8.2 Abbreviations used in Figure 3.4.3.2.1. to Figure 3.4.3.2.2.

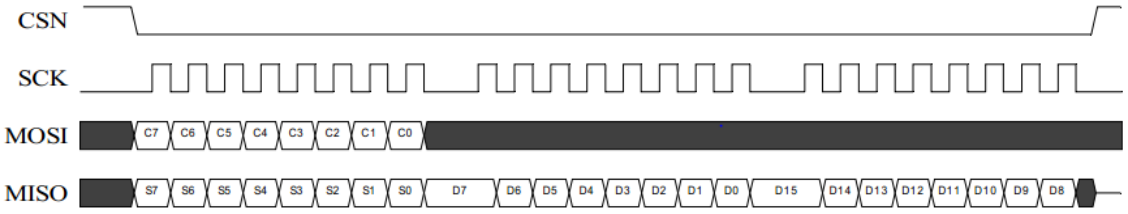


Figure 3.4.3.2.1 SPI read operation

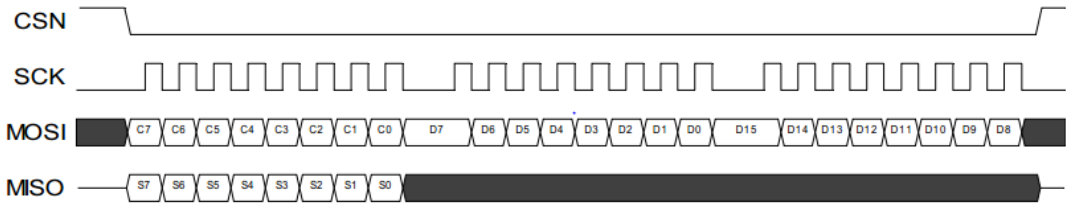


Figure 3.4.3.2.2 SPI write operation

3.4.4 Data FIFO

The data FIFOs store transmitted payloads (TX FIFO) or received payloads that are ready to be clocked out (RX FIFO). The FIFOs are accessible in both PTX mode and PRX mode. The following FIFOs are present in the RF transceiver:

- TX three level, 32 byte FIFO
- RX three level, 32 byte FIFO

Both FIFOs have a controller and are accessible through the SPI by using dedicated SPI commands. A TX FIFO in PRX can store payloads for ACK packets to three different PTX devices. If the TX FIFO contains more than one payload to a pipe, payloads are handled using the first in – first out principle. The TX FIFO in a PRX is blocked if all pending payloads are addressed to pipes where the link to the PTX is lost. In this case, the MCU can flush the TX FIFO using the FLUSH_TX command.

The RX FIFO in PRX can contain payloads from up to three different PTX devices and a TX FIFO in PTX can have up to three payloads stored.

You can write to the TX FIFO using these three commands; W_TX_PAYLOAD and W_TX_PAYLOAD_NO_ACK in PTX mode and W_ACK_PAYLOAD in PRX mode. All three commands provide access to the TX_PLD register.

The RX FIFO can be read by the command R_RX_PAYLOAD in PTX and PRX mode. This command provides access to the RX_PLD register.

The payload in TX FIFO in a PTX is not removed if the MAX_RT IRQ is asserted.

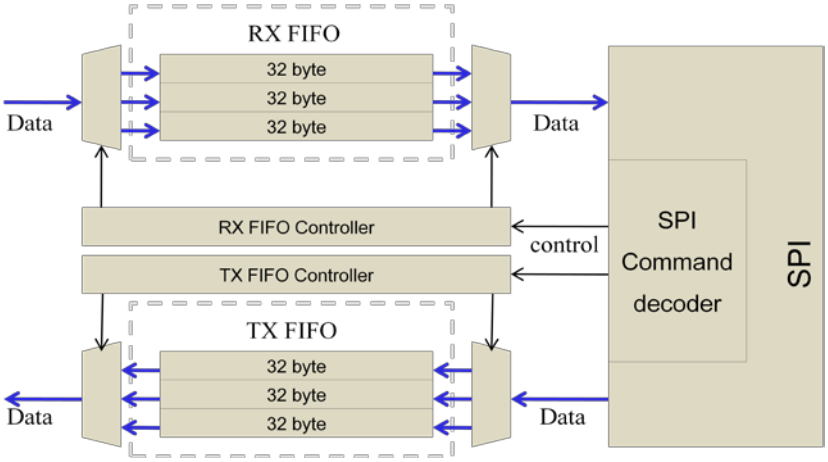


Figure 3.4.4 FIFO (RX and TX) block diagram

You can read if the TX and RX FIFO are full or empty in the FIFO_STATUS register.

3.4.5 Interrupt

The RF has an active low interrupt (IRQ) pin. The IRQ pin is activated when TX_DS IRQ, RX_DR IRQ or MAX_RT IRQ are set high by the state machine in the STATUS register. The IRQ pin resets when MCU writes '1' to the IRQ source bit in the STATUS register. The IRQ mask in the CONFIG register is used to select the IRQ sources that are allowed to assert the IRQ pin. By setting one of the MASK bits high, the corresponding IRQ source is disabled. By default all IRQ sources are enabled.

Note: The 3 bit pipe information in the STATUS register is updated during the IRQ high to low transition. The pipe information is unreliable if the STATUS register is read during an IRQ high to low transition.

3.5 Register map

You can configure and control the radio by accessing the register map through the SPI.

3.5.1 Register map table

All undefined bits in the table below are redundant. They are read out as '0'.

Note: Addresses 18 to 1B are reserved for test purpose, alteringthem makes the chip malfunction.

3.5.1.1 CONFIG (RW) Address: 00h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	MASK_RX_DR	MASK_TX_DS	MASK_MAX_RT	EN_CRC	CRCO	PWR_UP	PRIM_RX
0	0	0	0	1	0	0	0
RW	RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description	
7	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
6	0	MASK_RX_DR	Mask interrupt caused by RX_DR	
			0	Reflect RX_DR as active low interrupt on the IRQ pin
			1	Interruptnot reflected on the IRQ pin
5	0	MASK_TX_DS	Mask interrupt caused by TX_DS	
			0	Reflect TX_DS as active low interrupt on the IRQ pin
			1	Interrupt not reflected on the IRQpin
4	0	MASK_MAX_RT	Mask interrupt caused by MAX_RT	
			0	Reflect MAX_RT as active low interrupt on the IRQ pin
			1	Interrupt not reflected on the IRQ pin
3	1	EN_CRC	Enable CRC. Forced high if one of the bits in the EN_AA is high	
			0	Disable CRC
			1	Enable CRC
2	0	CRCO	CRC encoding scheme	
			0	1 byte
			1	2 byte
1	0	PWR_UP	Power up control	
			0	POWER DOWN
			1	POWER UP
0	0	PRIM_RX	RX/TX control	
			0	PTX
			1	PRX

3.5.1.2 EN_AA (RW) Address: 01h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reversed		ENAA_P5	ENAA_P4	ENAA_P3	ENAA_P2	ENAA_P1	ENAA_P0
0		1	1	1	1	1	1
RW		RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description	
7	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
6	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5	1	ENAA_P5	Enable auto acknowledgement data pipe 5	
			0	Disable
			1	Enable
4	1	ENAA_P4	Enable auto acknowledgement data pipe 4	
			0	Disable
			1	Enable
3	1	ENAA_P3	Enable auto acknowledgement data pipe 3	
			0	Disable
			1	Enable
2	1	ENAA_P2	Enable auto acknowledgement data pipe 2	
			0	Disable
			1	Enable
1	1	ENAA_P1	Enable auto acknowledgement data pipe 1	
			0	Disable
			1	Enable
0	1	ENAA_P0	Enable auto acknowledgement data pipe 0	
			0	Disable
			1	Enable

3.5.1.3 EN_RXADDR (RW) Address: 02h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reversed		ERX_P5	ERX_P4	ERX_P3	ERX_P2	ERX_P1	ERX_P0
0		0	0	0	0	1	1
RW		RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description	
7:6	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5	0	ERX_P5	Enable data pipe 5	
			0	Disable
			1	Enable
4	0	ERX_P4	Enable data pipe 4	
			0	Disable
			1	Enable
3	0	ERX_P3	Enable data pipe 3	
			0	Disable
			1	Enable
2	0	ERX_P2	Enable data pipe 2	
			0	Disable
			1	Enable
1	1	ERX_P1	Enable data pipe 1	
			0	Disable
			1	Enable
0	1	ERX_P0	Enable data pipe 0	
			0	Disable
			1	Enable

3.5.1.4 SETUP_AW (RW)Address: 03h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved						SETUP_AW	
0						2’b11	

RW	RW

Description of Word

Bit	Value	Symbol	Description	
7:2	0	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
1:0	2'b11	SETUP_AW	Setup of Address Widths (common for all data pipes)	
			2'b11	5 bytes
			2'b10	4 bytes
			2'b01	Illegal
			2'b00	Illegal

3.5.1.5 SETUP_RETR (RW) Address: 04h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ARD				ARC			
4'b0				4'b11			
RW				RW			

Description of Word

Bit	Value	Symbol	Description	
7:2	4'b0	ARD	Auto Retransmit Delay	
			4'hf	Wait 3840μS
			…	…
			4'h1	Wait 256μS
			4'h0	Wait 0μS
3:0	4'b11	ARC	Auto Retransmit Count	
			4'hf	Up to 15 Re-Transmit on fail of AA
			…	…
			4'h1	Up to 1 Re-Transmit on fail of AA
			4'h0	Re-Transmit disabled

3.5.1.6 RF_CH (RW) Address: 05h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reg_Rf_ch							
8'b2							
RW							

Description of Word

Bit	Value	Symbol	Description
8:0	2	Reg_Rf_ch	Sets the frequency channel RF operates on

3.5.1.7 RF_SETUP (RW) Address: 06h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONT_WAVE	PA_PWR[3]	RF_DR_LOW	Reserved	RF_DR_HIGH	PA_PWR		
0	1	0	0	1	3'b010		
RW	RW	RW	RW	RW	RW		

Description of Word

Bit	Value	Symbol	Description
7	0	CONT_WAV	Enables continuous carrier transmit when high

		E	0	Disable
			1	Enable
6	1	PA_PWR[3]	PA power select bit 3	
5	0	RF_DR_LOW	See RF_DR_HIGH for encoding.	
4	0	reserved	Reserved	
3	1	RF_DR_HIGH	Select between the high speed data rates. This bit is donot care if RF_DR_LOW is set.Encoding: [RF_DR_LOW, RF_DR_HIGH]:	
			11	500Kbps
			10	reserved
			01	2Mbps
			00	1Mbps
2:0	3'b010	PA_PWR[2:0]	PA power control, PA_PWR[3:0] with pa_voltage of RF_IVGEN in bank1	
			PA_PWR[3:0]	Pa_voltage(bank1 of RF_IVGEN)
			1111	0
			1000	0
			0111	1
			0011	0
			0001	0
			0001	1
			0000	0
			0000	1

			0111	Output 4 dbm, 25mA
			0011	Output 0 dbm, 18.5mA
			0001	Output -6 dbm
			0001	Output -12 dbm
			0000	Output -16 dbm
			0000	Output -43 dbm

3.5.1.8 STATUS (RW) Address: 07h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BANK	RX_DR	TX_DS	MAX_RT	RX_P_NO			TX_FULL
0	0	0	0	3'b111			0
R	RW	RW	RW	R			R

Description of Word

Bit	Value	Symbol	Description	
7	0	BANK	Register BANK status	
			1	Register R/W is to register BANK1
			0	Register R/W is to register BANK0
6	0	RX_DR	Data Ready RX FIFO interrupt. Asserted when new data arrives RX FIFO Write 1 to clear bit.	
5	0	TX_DS	Data Sent TX FIFO interrupt. Asserted when packet transmitted on TX. If AUTO_ACK isactivated, this bit is set high only when ACK is received. Write 1 to clear bit.	
4	0	MAX_RT	Maximum number of TX retransmits interrupt, Write 1 to clear bit. If MAX_RT is asserted it must be cleared to enable further communication.	
3:1	3'b111	RX_P_NO	Data pipe number for the payload available for reading from RX_FIFO	
			111	RX FIFO Empty
			110	Not Used
			000-101	Data Pipe Number
0	0	TX_FULL	TX FIFO full flag	
			0	Available locations in TX FIFO
			1	TX FIFO full

3.5.1.9 OBSERVE_TX (RW) Address: 08h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLOS_CNT				ARC_CNT			
4'h0				4'h0			
R				R			

Description of Word

Bit	Value	Symbol	Description
7:4	4'h0	PLOS_CNT	Count lost packets. The counter is overflow protected to 15, and discontinues at max until reset. The counter is reset by writing to RF_CH.
3:0	4'h0	ARC_CNT	Count retransmitted packets. The counter is reset when transmission of a new packet starts.

3.5.1.10 RPD Address: 09h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
sig_dbm_est							
8'h0							
R							

Description of Word

Bit	Value	Symbol	Description	
7:0	0	sig_dbm_est	estimated in-band signal level in dBm, should support -100 ~ +10 dBm,	
			11000000	-64 dBm

3.5.1.11 RX_ADDR_P0 (RW) Address: 0Ah

Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32
RX_ADDR_P0							
8'h70							
RW							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
RX_ADDR_P0							
8'h41							
RW							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
RX_ADDR_P0							
8'h88							
RW							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
RX_ADDR_P0							
8'h20							
RW							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P0							
8'h46							
RW							

Description of Word

Bit	Value	Symbol	Description
39:0	40'7041882046	RX_ADDR_P0	Receive address data pipe 0. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)

3.5.1.12 RX_ADDR_P1 (RW) Address: 0Bh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P1							
8'Hc2							

RW

Description of Word

Bit	Value	Symbol	Description
7:0	8'hc2	RX_ADDR_P1	Receive address data pipe 2. Only LSB. MSBytes are equal to RX_ADDR_P0[39:8]

3.5.1.13 RX_ADDR_P2 (RW) Address: 0Ch

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P2							
8'Hc3							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	8'hc3	RX_ADDR_P2	Receive address data pipe 2. Only LSB. MSBytes are equal to RX_ADDR_P0[39:8]

3.5.1.14 RX_ADDR_P3 (RW) Address: 0Dh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P3							
8'Hc4							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	8'hc4	RX_ADDR_P3	Receive address data pipe 3. Only LSB. MSBytes are equal to RX_ADDR_P0[39:8]

3.5.1.15 RX_ADDR_P4 (RW) Address: 0Eh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P4							
8'Hc5							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	8'hc5	RX_ADDR_P4	Receive address data pipe 4. Only LSB. MSBytes are equal to RX_ADDR_P0[39:8]

3.5.1.16 RX_ADDR_P5 (RW) Address: 0Fh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_ADDR_P5							
8'Hc6							
RW							

Description of Word

Bit	Value	Symbol	Description
7:0	8'hc6	RX_ADDR_P5	Receive address data pipe 5. Only LSB. MSBytes are equal to RX_ADDR_P0[39:8]

3.5.1.17 TX_ADDR(RW) Address: 10h

Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit 32

TX_ADDR							
8'h70							
RW							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
TX_ADDR							
8'h41							
RW							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
TX_ADDR							
8'h88							
RW							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
TX_ADDR							
8'h20							
RW							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
TX_ADDR							
8'h46							
RW							

Description of Word

Bit	Value	Symbol	Description
39:0	40'h7041882046	TX_ADDR	Transmit address. Used for a PTX device only. (LSByte is written first)Set RX_ADDR_P0 equal to this address to handle automatic acknowledge if this is a PTX device with Protocol engine enabled.

3.5.1.18 RX_PW_P0 (RW) Address: 11h

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Reserved		RX_PW_P0					
0		0					
RW		RW					

Description of Word

Bit	**Value**	**Symbol**	**Description**	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5:0	0	RX_PW_P0	Number of bytes in RX payload in data pipe 0 (1 to 32 bytes)	
			32	32 bytes
			…	…
			1	1 byte
			0	Pipe not used

3.5.1.19 RX_PW_P1 (RW) Address: 12h

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Reserved		RX_PW_P1					
0		0					
RW		RW					

Description of Word

Bit	Value	Symbol	Description	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5:0	0	RX_PW_P1	Number of bytes in RX payload in data pipe 1 (1 to 32 bytes)	
			32	32 bytes
			…	…
			1	1 byte
			0	Pipe not used

3.5.1.20 RX_PW_P2 (RW) Address: 13h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RX_PW_P2					
0		0					
RW		RW					

Description of Word

Bit	Value	Symbol	Description	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5:0	0	RX_PW_P2	Number of bytes in RX payload in data pipe 2 (1 to 32 bytes)	
			32	32 bytes
			…	…
			1	1 byte
			0	Pipe not used

3.5.1.21 RX_PW_P3 (RW) Address: 14h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RX_PW_P3					
0		0					
RW		RW					

Description of Word

Bit	Value	Symbol	Description	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5:0	0	RX_PW_P3	Number of bytes in RX payload in data pipe 3 (1 to 32 bytes)	
			32	32 bytes
			…	…
			1	1 byte
			0	Pipe not used

3.5.1.22 RX_PW_P4 (RW) Address: 15h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RX_PW_P4					
0		0					
RW		RW					

Description of Word

Bit	Value	Symbol	Description	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value

			1	Reset to default values
5:0	0	RX_PW_P4	Number of bytes in RX payload in data pipe 4 (1 to 32 bytes)	
			32	32 bytes
			…	…
			1	1 byte
			0	Pipe not used

3.5.1.23 RX_PW_P5 (RW) Address: 16h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved		RX_PW_P4					
0		0					
RW		RW					

Description of Word

Bit	Value	Symbol	Description	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5:0	0	RX_PW_P5	Number of bytes in RX payload in data pipe 5 (1 to 32 bytes)	
			32	32 bytes
			…	…
			1	1 byte
			0	Pipe not used

3.5.1.24 FIFO_STATUS (RW) Address: 17h

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	TX_REUSE_PL	TX_FULL	TX_EMPTY	Reserved		RX_FULL	RX_EMPTY
0	0	0	1	0		0	1
R	R	R	R	R		R	R

Description of Word

Bit	Value	Symbol	Description	
7	0	Reserved	Only '0' allowed	
			0	Keep the current value
			1	Reset to default values
6	0	TX_REUSE_PL	TX REUSE flag.	
			1	Tx data reused
			0	Tx data not reused
5	0	TX_FULL	TX FIFO full flag.	
			1	TX FIFO full
			0	Available locations in TX FIFO
4	1	TX_EMPTY	TX FIFO empty flag.	
			1	TX FIFO empty
			0	Data in TX FIFO
3:2	2'b00	Reserved	Only '00' allowed	
			0	Keep the current value
			1	Reset to default values
1	0	RX_FULL	RX FIFO full flag.	
			1	RX FIFO full
			0	Available locations in RX FIFO
0	1	RX_EMPTY	RX FIFO empty flag.	
			1	RX FIFO empty
			0	Data in RX FIFO

3.5.1.25 DYNPD (RW) Address: 1Ch

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Reserved	DPL_P5	DPL_P4	DPL_P3	DPL_P2	DPL_P1	DPL_P0
0	0	0	0	0	0	0
RW	RW	RW	RW	RW	RW	RW

Description of Word

Bit	Value	Symbol	Description	
7:6	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
5	0	DPL_P5	Enable dynamic payload length data pipe 5. (Requires EN_DPL)	
4	0	DPL_P4	Enable dynamic payload length data pipe 4. (Requires EN_DPL)	
3	0	DPL_P3	Enable dynamic payload length data pipe 3. (Requires EN_DPL)	
2	0	DPL_P2	Enable dynamic payload length data pipe 2. (Requires EN_DPL)	
1	0	DPL_P1	Enable dynamic payload length data pipe 1. (Requires EN_DPL)	
0	0	DPL_P0	Enable dynamic payload length data pipe 0. (Requires EN_DPL)	

3.5.1.26 FEATURE (RW) Address: 1Dh

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					EN_DPL	EN_ACK_PAY	EN_DYN_ACK
0					0	0	0
RW					RW	RW	RW

Description of Word

Bit	Value	Symbol	Description	
7:3	2'b00	Reserved	Only 0 allowed	
			0	Keep the current value
			1	Reset to default values
2	0	EN_DPL	Enables Dynamic Payload Length	
1	0	EN_ACK_PAY	Enables Payload with ACK	
0	0	EN_DYN_ACK	Enables the W_TX_PAYLOAD_NOACK command	

3.5.1.27 SETUP_VALUE (RW) Address: 1Eh

Bit 39	Bit 38	Bit 37	Bit 36	Bit 35	Bit 34	Bit 33	Bit32
REG_LNA_WAIT							
8'h00							
RW							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit24**
REG_MBG_WAIT							
8'h10							
RW							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
RX_TM_CNT							
8'h80							
RW							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
TX_SETUP_VALUE							
8'h32							
RW							

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_SETUP_VALUE							
8'h28							
RW							

Description of Word

Bit	Value	Symbol	Description	
39:32	8'h00	REG_LNA_WAIT	Lna wait counter	
			8'hff	255 cycle
			…	…
			1	1 cycle
			0	0 cycle
31:24	8'h10	REG_MBG_WAIT	Main bandgap wait counter	
			8'hff	255us
			…	…
			1	1 us
			0	0 us
23:16	8'h80	RX_TM_CNT	Rx timeout counter.	
			8'hff	255us
			…	…
			1	1 us
			0	0 us
15:8	8'h32	TX_SETUP_VALUE	TX_SETUP time, the time between Standby to TX mode	
			8'hff	255us
			…	…
			1	1 us
			0	0 us
7:0	8'h28	RX_SETUP_VALUE	RX_SETUP time, the time between Standby to RX mode	
			8'hff	255us
			…	…
			1	1 us
			0	0 us

3.5.1.28 PRE_GURD (RW) Address: 1Fh

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CE_REG	SPARE_REG[6:0]						
0	0						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TAIL_CTL			GRD_EN	GRD_CNT			
1			1	4'h2			
RW			RW	RW			

Description of Word

Bit	Value	Symbol	Description	
15	0	CE_REG	CE=CE_PAD&(~CE_REG)，when CE pad connected to power， CE_REG can be used to control CE	
14:8	0	SPARE_REG	Reserved register	
7:5	1	TAIL_CTL	Number of repeat bit after the CRC	
			7	7 repeat tail
			…	…
			1	1 repeat tail
			0	0 No repeat tail
4	1	GRD_EN	Pre-Guard enable	
3:0	4’h2	GRD_CNT	Number of Pre-Guard bit before preamble	
			4’hf	16 bit pre_guard
			…	…
			1	2 bit pre_guard
			0	1 bit pre_guard

4 Electrical Characteristics

4.1.1 Absolute Maximum Rating

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Supply Voltage	VDD-VSS	-0.3	+3.6	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Oscillator Frequency	1/TCLCL	2	25	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-40	+125	°C

Table 8.1.1 Absolute Maximum Rating

4.1.2 DC Electrical Characteristics

(Measurements condition: VDD=3.3V, TA=+25°C)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation Voltage	VDD	2.3	-	3.6	V	
Analog Operation Voltage	AVDD	2.3	-	3.6	V	
Input High Voltage P0/1/2/3	VIH	2.1	-	VDD + 0.2	V	VDD=3.3V
Input Low Voltage P0/1/2/3	VIL	-0.2	-	0.9	V	VDD=3.3V
Input High Voltage XTAL	VIHX	2.1	-	VDD + 0.2	V	VDD=3.3V
Input Low Voltage XTAL	VILX	-0.2	-	0.9	V	VDD=3.3V
Input High Voltage RESET (Schmitt input)	VIHR	2.0	-	VDD + 0.2	V	VDD=3.3V
Input Low Voltage RESET (Schmitt input)	VIHR	-0.2	-	1.0	V	VDD=3.3V
Sink current P0/1/2/3 (Quasi-bidirectional and push-pull	ISK	-	10	-	mA	VDD=3.3V
Source current P0/1/2/3 (Quasi-bidirectional Mode)	ISRQ	-	200	-	uA	VDD=3.3V, Vo=2.4V
Source current P0/1/2/3 (Push-pull Mode)	ISRP	-	5	-	mA	VDD=3.3V, Vo=2.7V
Reset Voltage of POR and LVR	VPOR	-	1.9	-	V	VDD=3.3V

Table 8.2.1 DC Electrical Characteristics

MCU normal mode		
MCU	**RF**	**Current**
@IRC 22MHz, VDD=3.3V, enable all IP	tx@8dBm	51 mA
	rx	31 mA
	standby_1	12 mA
	power_down	12 mA
@IRC 22MHz, VDD=3.3V, disable all APB clock	tx@8dBm	49 mA
	rx	29 mA
	standby_1	10 mA
	power_down	10 mA
@IRC 12MHz, VDD=3.3V, enable all IP	tx@8dBm	47 mA
	rx	26 mA
	standby_1	7 mA
	power_down	7 mA
@IRC 12MHz, VDD=3.3V, disable all APB clock	tx@8dBm	46mA
	rx	25mA
	standby_1	6mA
	power_down	6mA
@IRC 2MHz, VDD=3.3V, enable all IP	tx@8dBm	43 mA
	rx	21 mA
	standby_1	2 mA
	power_down	2 mA
@IRC 2MHz, VDD=3.3V, disable all APB clock	tx@8dBm	43 mA
	rx	21 mA
	standby_1	2 mA
	power_down	2mA
MCU sleep mode		
WFI@IRC 10kHz, VDD=3.3V, disable all APB clock	tx@8dBm	41 mA
WFI@IRC 10kHz, VDD=3.3V, disable all APB clock	rx	20 mA
WFI@IRC 10kHz, VDD=3.3V, disable all APB clock	standby_1	184uA
WFI@IRC 10kHz, VDD=3.3V, disable all APB clock	power_down	160 uA
MCU deep sleep mode		
Deep power down	power_down	16uA

4.1.3 AC Electrical Characteristics

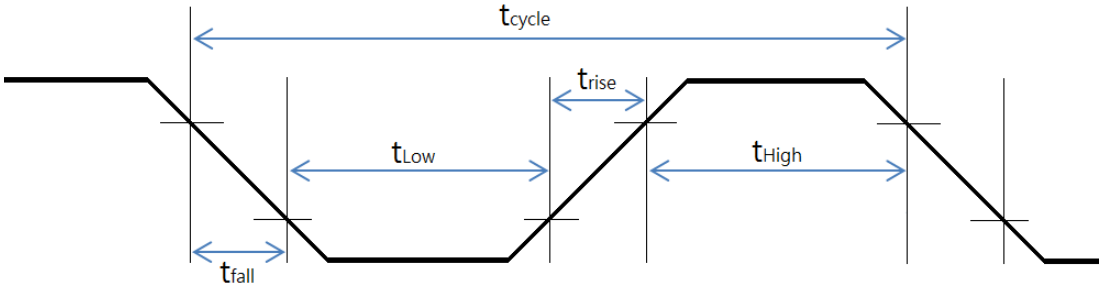


Figure 4.1.3 AC Electrical Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Clock High Time	tHigh	20	-	-	ns	@ 25MHz XTAL
Clock Low Time	tLow	20	-	-	ns	@ 25MHz XTAL
Clock Rise Time	trise	-	-	10	ns	@ 25MHz XTAL
Clock Fall Time	tfall	-	-	10	ns	@ 25MHz XTAL

Table 4.1.3 AC Electrical Characteristics

4.1.4 Rf performance

4.1.4.1 Receiver performance

No.	Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
1	Max RX signal	Pin,max	<0.1% BER		-10		dBm
2	500Kbps	Sensitivity	<0.1%BER		-88		dBm
3	1Mbps	Sensitivity	<0.1%BER		-88		dBm
4	2Mbps	Sensitivity	<0.1%BER		-83		dBm

Table 4.1.4.1 RF Receiver performance

4.1.4.2 Transmitter performance

No.	Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
1	Max Output Power	Pmax	50ohm antenna		0	+6	dBm
2	Min Output Power	Pmin	50ohm antenna		-16		dBm
3	RF power control range	Prange	50ohm antenna		22		dB

Table 4.1.4.2 RF Transmitter performance

4.1.5 ypical Crystal

4.1.5.1 typical Crystal for M0

Crystal	CLX1	CLX2
2MHz ~ 25MHz	Optional (Depend on crystal specification)	

Table 4.1.5.1 Typical Crystal for M0

4.1.5.2 typical Crystal for RF

No.	Parameter	Symbol	Conditions	MIN	TYP	MAX	UNIT
1	Crystal Frequency	Fxtal		16	16	16	MHz
2	Tolerance	Dfxtal		-60		+60	ppm
3	Load capacitance	Cxtal			12		Pf

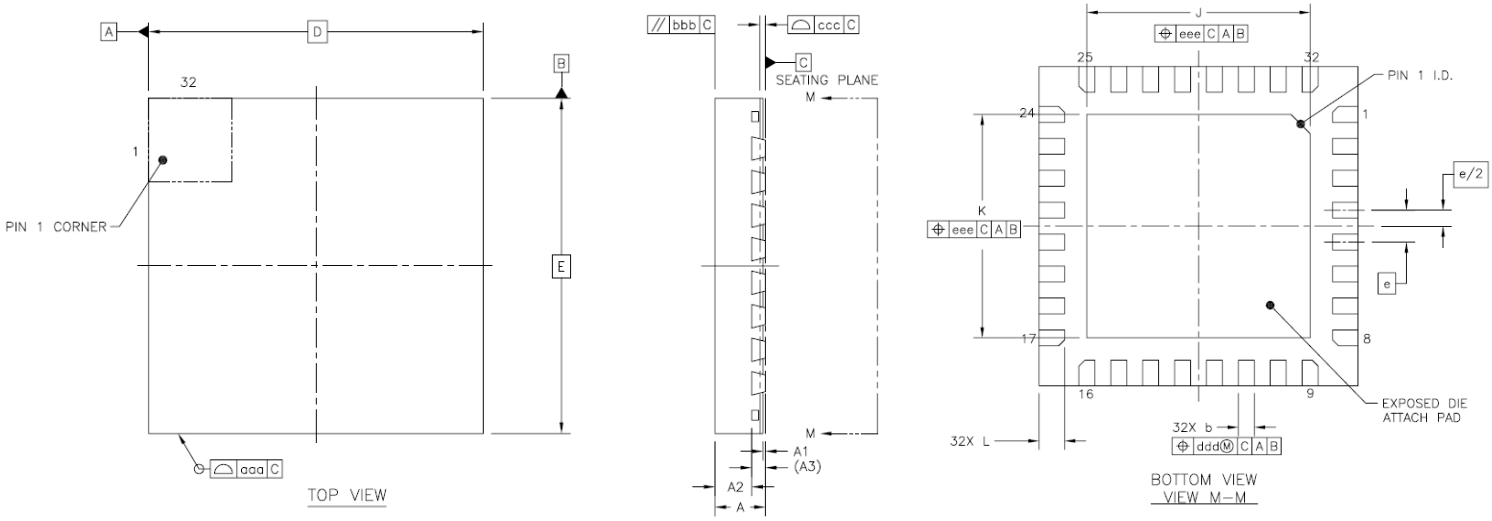
Table 4.1.5.2 typical Crystal for RF

4.1.6 Analog to digital conversion

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Resolution	-	-	-	12	Bit
Differential nonlinearity error	DNL	-	-	1	LSB
Integral nonlinearity error	INL	-	-	2	LSB
Input Voltage Range	-	0.01*AVDD	-	0.99* AVDD	V
ADC clock frequency	FADC	-	-	3.2	MHz
Sample Time	TS	-	-	200	kS/s
Conversion time	TADC	-	16	-	Clock
Input capacitance	CIN	-	5.12	-	pF

Table 4.1.6 Analog to digital conversion

5 Package Information



DESCRIPTION		SYMBOL	MILLIMETER		
			MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	